1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-07-23

SCHEM,MLB,K16

07/23/2010

Page (.csa)		Contents	Sync	Date
1	1	Table of Contents	N/A	N/A
2	2	System Block Diagram	ALAN.DAI	02/26/2010
3	3	Power Block Diagram	MARTIN.YEH	2/25/2010
4	4	BOM Configuration	K6_MLB	12/11/2009
5	5	K16 BOM Variants	N/A	N/A
6	6	Revision History	N/A	N/A
7	7	Functional Test / No Test	(K99_MLB)	(02/16/2010)
8	8	Power Aliases	(K99_MLB)	(02/11/2010)
9	9	Signal Aliases	(MASTER)	(MASTER)
10	10	CPU FSB	K99_MLB	04/08/2010
11	11	CPU Power & Ground	K99_MLB	04/08/2010
12	12	CPU Decoupling & VID	(K99_MLB)	(02/11/2010)
13	13	eXtended Debug Port (Micro-XDP)	K99_MLB	03/01/2010
14	14	MCP CPU Interface	K99_MLB	04/08/2010
15	15	MCP Memory Interface	K99_MLB	04/08/2010
16	16	MCP PCIe Interfaces	K99_MLB	04/08/2010
17	17	MCP Graphics	K99_MLB	04/08/2010
18	18	MCP SATA, USB & Ethernet	K99_MLB	04/08/2010
19	19	MCP HDA, LPC & MISC	K99_MLB	04/08/2010
20	20	MCP Power & Ground	K99_MLB	04/08/2010
21	23	MCP89 Memory Rail Gating	K99_MLB	04/08/2010
22	24	MCP89 GFX Core Rail Gating	K99_MLB	04/08/2010
23	25	MCP Standard Decoupling	K99_MLB	04/08/2010
24	26	MCP Graphics Support	K99_MLB	04/08/2010
25	28	SB Misc	(K99_MLB)	(02/11/2010)
26	31	DDR3 DRAM Channel A (0-31)	K99_MLB	04/08/2010
27	32	DDR3 DRAM Channel A (32-63)	K99_MLB	04/08/2010
28	33	DDR3 DRAM Channel B (0-31)	K99_MLB	04/08/2010
29	34	DDR3 DRAM Channel B (32-63)	K99_MLB	04/08/2010
30	35	DDR BYPASSING 1	K99_MLB	04/08/2010
31	36	DDR BYPASSING 2	K99_MLB	04/08/2010
32	37	Memory Active Termination	K99_MLB	04/08/2010
33	39	FSB/DDR3 Vref Margining	K99_MLB	04/08/2010
34	40	X21 WIRELESS CONNECTOR	K99_MLB	04/08/2010
35	45	SATA CONNECTOR	K99_MLB	04/08/2010
36	46	External USB Connectors	K99_MLB	03/01/2010
37	47	Left I/O (LIO) Connector	(MASTER)	(MASTER)
38	48	SecureDigital Card Reader	(MASTER)	(MASTER)
39	49	SMC	K16_MLB	06/01/2010
40	50	SMC Support	(K99_MLB)	(03/01/2010)
41	51	LPC+SPI Debug Connector	K99_MLB	04/08/2010
42	52	K16/K99 SMus Connections	K99_MLB	07/23/2010
43	53	Voltage & Current Sensing	K99_MLB	04/08/2010
44	54	Current Sensing	K99_MLB	04/08/2010
45	55	Thermal Sensors	K99_MLB	04/08/2010
46	56	Fan	K99_MLB	04/08/2010
47	57	WELLSPRING 1	K99_MLB	04/08/2010
48	61	SPI ROM	K99_MLB	04/08/2010
49	66	AUDI0: SPEAKER AMP	K99_MLB	04/08/2010
50	69	DC-In & Battery Connectors	(MASTER)	(MASTER)
51	70	PBus Supply & Battery Charger	(K99_MLB)	(02/16/2010)
52	72	5V / 3.3V Power Supply	K99_MLB	04/08/2010
53	73	1.5V/1.35V LVDDR3 Supply	K16_MLB	06/01/2010
54	74	IMVP6 CPU VCore Regulator	(K99_MLB)	(02/16/2010)
55	75	MCP VCore Regulator	(K99_MLB)	(02/11/2010)
56	76	CPUVTT (1.05V) Power Supply	(K99_MLB)	(03/01/2010)
57	77	Misc Power Supplies	K99_MLB	04/08/2010
58	78	Power Sequencing	K99_MLB	04/08/2010
59	79	Power FETs	K99_MLB	04/08/2010
60	90	Internal DisplayPort Connector	K99_MLB	07/23/2010
61	93	External DisplayPort Support	K99_MLB	04/08/2010
62	94	DisplayPort Connector	K16_MLB	06/01/2010
63	97	LCD Backlight Driver	(K99_MLB)	(03/01/2010)
64	98	LCD Backlight Support	K99_MLB	04/08/2010
65	99	Additional CPU/GPU Decoupling	K99_MLB	05/18/2010
66	100	CPU/FSB Constraints	K99_MLB	04/08/2010
67	101	Memory Constraints	K99_MLB	04/08/2010
68	102	MCP Constraints 1	K99_MLB	04/08/2010
69	103	MCP Constraints 2	K99_MLB	04/08/2010
70	104	Ethernet Constraints	K99_MLB	04/08/2010
71	106	SMC Constraints	K99_MLB	04/08/2010
72	108	K16/K99 Specific Constraints	T27_MLB	09/08/2009
73	109	K99 RULE DEFINITIONS	K99_MLB	04/08/2010
74	110	Acoustic Cap BOM Config Tables	K16_MLB	06/01/2010

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8467	1	SCHEM,MLB,K16	SCH	CRITICAL	
820-2838	1	PCBF,MLB,K16	PCB	CRITICAL	

DRAWING TITLE: SCHEM,MLB,K16

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

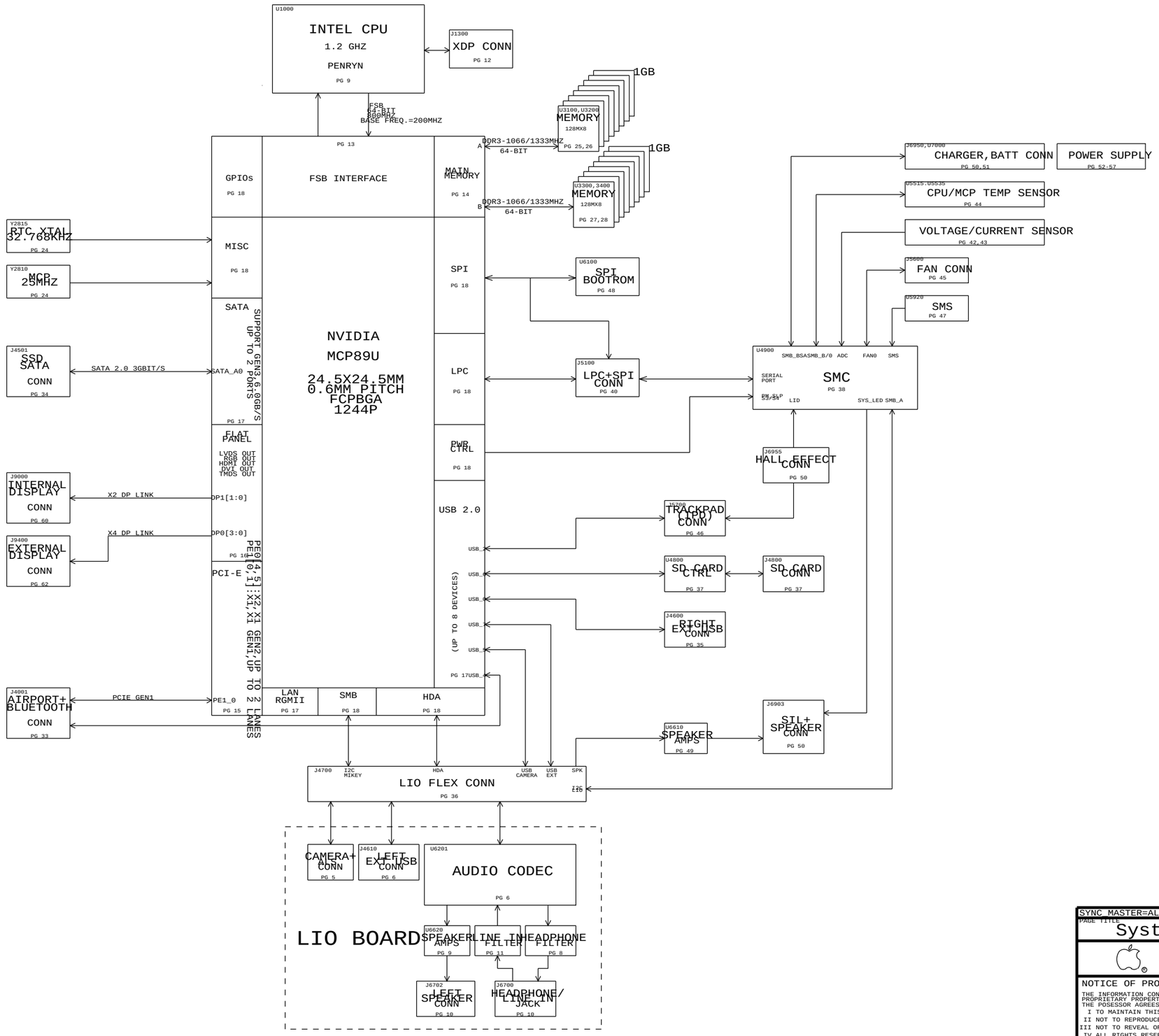
BRANCH:

PAGE: 1 OF 110

SHEET: 1 OF 74

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=ALAN.DAI SYNC_DATE=02/26/2010

PAGE TITLE
System Block Diagram

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

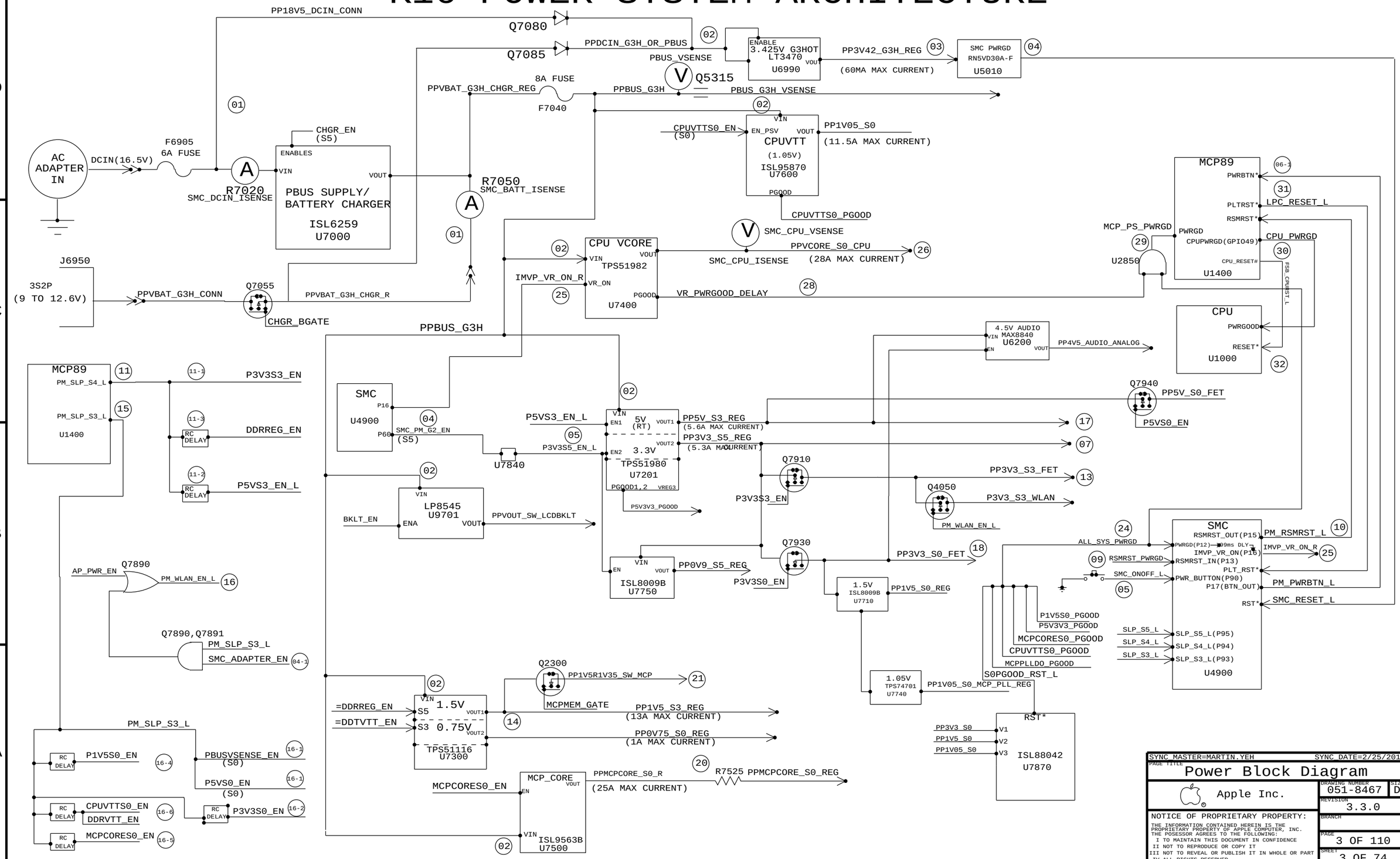
BRANCH

PAGE 2 OF 110

SHEET 2 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

K16 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=MARTIN.YEH SYNC_DATE=2/25/2010

PAGE TITLE

Power Block Diagram

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

PAGE 3 OF 110

SHEET 3 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

K16 BOM Variants on following page

DRAM CFG CHART

VENDOR	CFG 0	CFG 1
HYNIX	0	0
SAMSUNG	0	1
MICRON	1	0
ELPIDA	1	1

SIZE	CFG 2
2GB	0
4GB	1

DIE REV	CFG 3
A	0
B	1

BOM Groups

BOM GROUP	BOM OPTIONS
K16_COMMON	COMMON,ALTERNATE,PROJ:K16,K16_MISC,MCP89U:A03,K16_DEBUG:ENG,K16_PROGPARTS,SPI:41MHZ,LVDDR3:YES,WLAN_PCTL:HW,IPD_5V:S5_INT,IPD_3V3:S5
K16_MISC	DP_ESD,DP_PWR:SMC,VFRQ:SLPS3,HVDDLDO:FIXED,MCPHVDD:P2V5,MCPPLL_R:REG,S0PGOOD_BJT,ISL6259_SCREENED:YES,DPI2C:SMC
K16_PROGPARTS	BOOTROM:UNLOCKED,SMC:PROG
K16_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,LPCPLUS,VREFMRGN:YES,EFI_DEBUG,S0PGOOD_ISL,MCPPLL_LDO,S3_S0_LED
K16_DEVEL:PVT	LPCPLUS
K16_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG:YES,XDP
K16_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
K16_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_2GB	DRAM_CFG0:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_2GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_4GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:MICRON_4GB
CAPS:SS	SS_CAP_2_2UF,SS_CAP_10UF,SS_CAP_1UF,SS_CAP_22UF
CAPS:MU	MU_CAP_2_2UF,MU_CAP_10UF,MU_CAP_1UF,MU_CAP_22UF
CAPS:TY	TY_CAP_2_2UF,TY_CAP_10UF,TY_CAP_1UF,TY_CAP_22UF

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC:BLANK
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM:BLANK

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0681	138S0638		ALL	TAIYO YUDEN AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
353S2987	353S2988	HVDDLDO:FIXED	ALL	TPS71725 ALTERNATE FOR U2590
104S0023	104S0018		ALL	CYNTEC/DALE AS ALTERNATES
107S0139	107S0075		ALL	CYNTEC AS ALTERNATE
138S0671	138S0673		ALL	TAIYO AS ALTERNATE
155S0578	155S0367		ALL	TAIYO AS ALTERNATE
376S0926	376S0610		ALL	FAIRCHILD AS ALTERNATE
155S0457	155S0329		ALL	MAGLAYERS AS ALTERNATE
377S0107	377S0066		ALL	ON SEMI AS ALTERNATE

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3820	1	IC,MCP89U-A01,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A01
337S3868	1	IC,MCP89U-A02,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A02
337S3938	1	IC,MCP89U-A03,24.5MMX24.5MM,1244FCBGA	U1400	CRITICAL	MCP89U:A03
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0552	4	HYNIX,LVDDR3,1GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0553	4	SAMSUNG,LVDDR3,1GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0554	4	MICRON,LVDDR3,1GBIT,8X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0565	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_2GB
333S0566	4	ELPIDA,LVDDR3,1GBIT,7.5X10.6	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,7.5X10.6	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,7.5X10.6	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0566	4	ELPIDA,LVDDR3,2GBIT,7.5X10.6	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0555	4	HYNIX,LVDDR3,2GBIT,9X11.1	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0556	4	SAMSUNG,LVDDR3,2GBIT,7.5X11.0	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_TYPE:MICRON_4GB
333S0557	4	MICRON,LVDDR3,2GBIT,9X11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_TYPE:MICRON_4GB
353S2392	1	IC,ISL6259,BATCHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:NO
353S2929	1	IC,ISL6259,BATCHARGER,3%,4C4MM,QFN28	U7000	CRITICAL	ISL6259_SCREENED:YES

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 4 OF 110
SHEET 4 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1070	PCBA,MLB,1.86GHZ HY 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWQ,CAPS:MU,DDR3:HYNIX_2GB
639-0837	PCBA,MLB,1.86GHZ,HY 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXW,CAPS:SS,DDR3:HYNIX_2GB
639-1096	PCBA,MLB,1.86GHZ HY 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXN,CAPS:TY,DDR3:HYNIX_2GB
639-1101	PCBA,MLB,1.86GHZ HY 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXV,CAPS:MU,DDR3:HYNIX_4GB
639-1098	PCBA,MLB,1.86GHZ HY 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXQ,CAPS:SS,DDR3:HYNIX_4GB
639-1068	PCBA,MLB,1.86GHZ HY 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWN,CAPS:TY,DDR3:HYNIX_4GB
639-1083	PCBA,MLB,1.86GHZ MI 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX6,CAPS:MU,DDR3:MICRON_2GB
639-1078	PCBA,MLB,1.86GHZ MI 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX1,CAPS:SS,DDR3:MICRON_2GB
639-1090	PCBA,MLB,1.86GHZ MI 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXG,CAPS:TY,DDR3:MICRON_2GB
639-1088	PCBA,MLB,1.86GHZ MI 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXD,CAPS:MU,DDR3:MICRON_4GB
639-1067	PCBA,MLB,1.86GHZ MI 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWM,CAPS:SS,DDR3:MICRON_4GB
639-1077	PCBA,MLB,1.86GHZ MI 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX0,CAPS:TY,DDR3:MICRON_4GB
639-1080	PCBA,MLB,1.86GHZ SA 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX3,CAPS:MU,DDR3:SAMSUNG_2GB
639-1095	PCBA,MLB,1.86GHZ SA 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXM,CAPS:SS,DDR3:SAMSUNG_2GB
639-1071	PCBA,MLB,1.86GHZ SA 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWR,CAPS:TY,DDR3:SAMSUNG_2GB
639-1097	PCBA,MLB,1.86GHZ SA 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXP,CAPS:MU,DDR3:SAMSUNG_4GB
639-1084	PCBA,MLB,1.86GHZ SA 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX7,CAPS:SS,DDR3:SAMSUNG_4GB
639-1091	PCBA,MLB,1.86GHZ SA 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXH,CAPS:TY,DDR3:SAMSUNG_4GB
639-1092	PCBA,MLB,2.13GHZ HY 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXJ,CAPS:MU,DDR3:HYNIX_2GB
639-1082	PCBA,MLB,2.13GHZ,HY 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX5,CAPS:SS,DDR3:HYNIX_2GB
639-1085	PCBA,MLB,2.13GHZ HY 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX8,CAPS:TY,DDR3:HYNIX_2GB
639-1089	PCBA,MLB,2.13GHZ HY 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXF,CAPS:MU,DDR3:HYNIX_4GB
639-1075	PCBA,MLB,2.13GHZ HY 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWX,CAPS:SS,DDR3:HYNIX_4GB
639-1079	PCBA,MLB,2.13GHZ HY 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX2,CAPS:TY,DDR3:HYNIX_4GB
639-1099	PCBA,MLB,2.13GHZ MI 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXR,CAPS:MU,DDR3:MICRON_2GB
639-1087	PCBA,MLB,2.13GHZ MI 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXC,CAPS:SS,DDR3:MICRON_2GB
639-1069	PCBA,MLB,2.13GHZ MI 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWP,CAPS:TY,DDR3:MICRON_2GB
639-1100	PCBA,MLB,2.13GHZ MI 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXT,CAPS:MU,DDR3:MICRON_4GB
639-1093	PCBA,MLB,2.13GHZ MI 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXK,CAPS:SS,DDR3:MICRON_4GB
639-1076	PCBA,MLB,2.13GHZ MI 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWY,CAPS:TY,DDR3:MICRON_4GB
639-1074	PCBA,MLB,2.13GHZ SA 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWW,CAPS:MU,DDR3:SAMSUNG_2GB
639-1072	PCBA,MLB,2.13GHZ SA 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWT,CAPS:SS,DDR3:SAMSUNG_2GB
639-1086	PCBA,MLB,2.13GHZ SA 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX9,CAPS:TY,DDR3:SAMSUNG_2GB
639-1073	PCBA,MLB,2.13GHZ SA 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWV,CAPS:MU,DDR3:SAMSUNG_4GB
639-1081	PCBA,MLB,2.13GHZ SA 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX4,CAPS:SS,DDR3:SAMSUNG_4GB
639-1094	PCBA,MLB,2.13GHZ SA 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXL,CAPS:TY,DDR3:SAMSUNG_4GB
639-1450	PCBA,MLB,1.86GHZ EL 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG4W,CAPS:MU,DDR3:ELPIDA_2GB
639-1451	PCBA,MLB,1.86GHZ EL 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG4Y,CAPS:SS,DDR3:ELPIDA_2GB
639-1455	PCBA,MLB,1.86GHZ EL 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG53,CAPS:TY,DDR3:ELPIDA_2GB
639-1453	PCBA,MLB,2.13GHZ EL 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG51,CAPS:MU,DDR3:ELPIDA_2GB
639-1454	PCBA,MLB,2.13GHZ EL 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG52,CAPS:SS,DDR3:ELPIDA_2GB
639-1452	PCBA,MLB,2.13GHZ EL 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG50,CAPS:TY,DDR3:ELPIDA_2GB
639-1458	PCBA,MLB,1.86GHZ EL 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5P,CAPS:MU,DDR3:ELPIDA_4GB
639-1463	PCBA,MLB,1.86GHZ EL 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5W,CAPS:SS,DDR3:ELPIDA_4GB
639-1460	PCBA,MLB,1.86GHZ EL 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5T,CAPS:TY,DDR3:ELPIDA_4GB
639-1462	PCBA,MLB,2.13GHZ EL 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5Q,CAPS:MU,DDR3:ELPIDA_4GB
639-1459	PCBA,MLB,2.13GHZ EL 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5V,CAPS:SS,DDR3:ELPIDA_4GB
639-1461	PCBA,MLB,2.13GHZ EL 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5R,CAPS:TY,DDR3:ELPIDA_4GB
607-6915	CMN PTS,PCBA,MLB,K16	K16_COMMON
085-1327	K16 MLB DEVELOPMENT BOM	K16_DEVEL:ENG

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWM]	CRITICAL	EEEE:DCWM
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWN]	CRITICAL	EEEE:DCWN
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWP]	CRITICAL	EEEE:DCWP
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWQ]	CRITICAL	EEEE:DCWQ
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWR]	CRITICAL	EEEE:DCWR
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWT]	CRITICAL	EEEE:DCWT
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWV]	CRITICAL	EEEE:DCWV
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWW]	CRITICAL	EEEE:DCWW
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWX]	CRITICAL	EEEE:DCWX
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWY]	CRITICAL	EEEE:DCWY
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX0]	CRITICAL	EEEE:DCX0
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX1]	CRITICAL	EEEE:DCX1
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX2]	CRITICAL	EEEE:DCX2
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX3]	CRITICAL	EEEE:DCX3
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX4]	CRITICAL	EEEE:DCX4
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX5]	CRITICAL	EEEE:DCX5
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX6]	CRITICAL	EEEE:DCX6
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX7]	CRITICAL	EEEE:DCX7
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX8]	CRITICAL	EEEE:DCX8
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX9]	CRITICAL	EEEE:DCX9
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXC]	CRITICAL	EEEE:DCXC
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXD]	CRITICAL	EEEE:DCXD
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXF]	CRITICAL	EEEE:DCXF
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXG]	CRITICAL	EEEE:DCXG
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXH]	CRITICAL	EEEE:DCXH
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXJ]	CRITICAL	EEEE:DCXJ
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXK]	CRITICAL	EEEE:DCXK
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXL]	CRITICAL	EEEE:DCXL
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXM]	CRITICAL	EEEE:DCXM
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXN]	CRITICAL	EEEE:DCXN
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXP]	CRITICAL	EEEE:DCXP
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXQ]	CRITICAL	EEEE:DCXQ
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXR]	CRITICAL	EEEE:DCXR
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXT]	CRITICAL	EEEE:DCXT
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXV]	CRITICAL	EEEE:DCXV
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXW]	CRITICAL	EEEE:DCXW
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG4W]	CRITICAL	EEEE:DG4W
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG4Y]	CRITICAL	EEEE:DG4Y
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG53]	CRITICAL	EEEE:DG53
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG51]	CRITICAL	EEEE:DG51
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG52]	CRITICAL	EEEE:DG52
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG50]	CRITICAL	EEEE:DG50
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5P]	CRITICAL	EEEE:DG5P
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5W]	CRITICAL	EEEE:DG5W
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5T]	CRITICAL	EEEE:DG5T
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5Q]	CRITICAL	EEEE:DG5Q
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5V]	CRITICAL	EEEE:DG5V
825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5R]	CRITICAL	EEEE:DG5R

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	TY_CAP_2_2UF

K16-Specific BOM Tables

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3751	1	PDC,SLGAB,PRQ,1.86,17W,1066,ED,6M,BGA	U1000	CRITICAL	CPU:1.86GHZ
337S3758	1	PDC,SLGEQ,PRQ,2.13,17W,1066,ED,6M,BGA	U1000	CRITICAL	CPU:2.13GHZ
341T0276	1	IC ASSY,SMC EXTERNAL,K16	U4900	CRITICAL	SMC:PROG
341T0275	1	IC ASSY,EFI UNLOCKED,K16	U6100	CRITICAL	BOOTROM:UNLOCKED
341S2785	1	IC EFI ROM,PVT,LOCKED,K16	U6100	CRITICAL	BOOTROM:LOCKED

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1327	1	K16 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-6915	1	CMN PTS,PCBA,MLB,K16	CMNPTS	CRITICAL	K16_CMNPTS

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
K16 BOM Variants

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 5 OF 110
SHEET 5 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Revision History

Proto 0 (ECO #0000876215, v1.0.0, P4 change #210266, 03/16/2010)

v1.1.0 (P4 change #211399, 03/24/2010)

MCP:
7742015 - Added RC to DDC pass FETs to avoid glitch (pp. 7, 93).
7788138 - Added feedback divider and BOM tables for more HVDD LDOs (pp. 4, 25).
SMC:
7761747 - Added resistors to connect TCON to SMC or MCP SMBus (pp. 4, 52, 90).
7787883 - Added support for DP HPD wake / S4 state (pp. 4, 7, 8, 19, 49, 50, 78, 94).
SMS:
7765466 - Added S3 pull-up to SMS_INT_L to prevent leakage path (pp. 50, 59).
7769139 - Unstuffed SMS circuit (pg. 4).
General:
7787897 - Property/page fixes to reduce CheckPlus warnings/errors (pp. 7, 8, 12, 17, 74, 93, 108).

v1.2.0 (P4 change #211839, 03/26/2010)

USB:
7796626 - Changed port switch from TPS2052B to TPS2069 (pg. 46).
SMC:
7787883 - Added PLACE_NEAR property on R5022 to avoid stub (pg. 50).
SMBus:
7761747 - Added TCON I2C nets to FUNC_TEST list for J9000 (pg. 7).
Power:
7796648 - Changed DP and LCD power from PP3V3_S3 to PP3V3_S5 (pp. 8, 90).
7796658 - Changed backlight driver to E00 version (pg. 97).
BOM:
7796661 - Set up primary & alternate for power supply FET (pp. 4, 72).
7796654 - Consolidated SSM6N15FE to SSM6N37FE (pg. 48).
7796658 - Changed RCs on some SMC analog inputs (pg. 54).
7796683 - Stuffed RC on backlight driver PWM input (pg. 97).
General:
7796631 - Sorted BOM variants for easier verification (pg. 5).
7796631 - Cosmetic clean-up (pg. 76).

v1.3.0 (P4 change #212050, 03/26/2010)

SMBus:
7761747 - Added isolation FET and unstuffed series R’s on TCON I2C for now (pp. 4, 90, 108).
Power Supply:
7796661 - Removed alternate FET, made some FETs primary to other APN (pp. 4, 72, 73, 76).
7798425 - R/C value changes for 3.42V G3Hot power supply (pg. 69).
7798399 - R/C value changes for 5V/3.3V power supply (pg. 72).
7800179 - R value changes for CPU VCore power supply (pg. 74).
7798445 - R value changes for 0.9V S5 power supply (pg. 77).
7796658 - Changed backlight driver back to non-E00 version (pp. 4, 97).
BOM:
7796658 - Added alternates for two caps per GSM and removed unused alternates (pg. 4).
7798399 - Consolidated 100pF caps (pp. 74, 75).

v1.4.0 (P4 change #212757, 03/31/2010)

MCP SPI:
7809733 - Changed strapping to select 62.5MHz SPI bus frequency (pg. 4).
SMBus:
7796631 - Added XDP connection to SMBus aliases page (pp. 13, 52).
7808530 - Changed SMC ’MGMT’ SMBus pull-ups from 4.7K to 2K (pg. 52).
7761747 - Documented SMBus addresses for panel (pg. 52).
SD Card:
7800415 - Changed SD Card discharge R to more standard value (pg. 48).
Power Supplies:
7803283 - Changed 5V S3 regulator output from 5.02V to 5.12V nominal (pg. 72).
7809760 - Stuffed C9799 and clarified tables/BOMOPTIONs around these parts (pg. 97).

Proto 1 (ECO #0000884508, v2.0.0, P4 change #212783, 03/31/2010)

v2.1.0 (P4 change #??????, ??/??/2010)

BOM:
7796658 - Changed OMITs to OMIT_TABLEs (pp. 10-11, 14-20, 26, 31-36, 49, 61).

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE: Revision History
Apple Inc.
DRAWING NUMBER: 051-8467 SIZE: D
REVISION: 3.3.0
BRANCH:
PAGE: 6 OF 110
SHEET: 6 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST			
TRUE	PP3V3_WLAN_F	7 34 40	(Need 5 TPs)
TRUE	WIFI_EVENT_L	34 39 40	
TRUE	PCIE_AP_R2D_N	34 68	
TRUE	PCIE_AP_R2D_P	34 68	
TRUE	PCIE_CLK100M_AP_N	16 34 68	
TRUE	PCIE_CLK100M_AP_P	16 34 68	
TRUE	USB_BT_P	18 34 69	
TRUE	USB_BT_N	18 34 69	
TRUE	PCIE_AP_D2R_P	16 34 68	
TRUE	PCIE_AP_D2R_N	16 34 68	
TRUE	PCIE_WAKE_L	16 34	
TRUE	AP_RESET_CONN_L	34	
TRUE	AP_CLKREQ_Q_L	34	
TRUE	=PP3V3_S3_BT	8 34	

(Need to add 6 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST			
TRUE	PP3V3_S0_HDD_R	7 35	(Need 5 TPs)
TRUE	SATA_HDD_D2R_C_P	35 68	
TRUE	SATA_HDD_D2R_C_N	35 68	
TRUE	SATA_HDD_R2D_N	35 68	
TRUE	SATA_HDD_R2D_P	35 68	
TRUE	SMC_HDD_OOB_TEMP	35 39	
TRUE	SMC_HDD_TEMP_CTL	35 39	

(Need to add 6 GND TPs)

J4700: LIO Connector

FUNC_TEST			
TRUE	=PP3V42_G3H_ONEWIRE	8 37	
TRUE	=PP3V3_S0_AUDIO	8 37	(Need 2 TPs)
TRUE	=PP1V8R1V5_S0_AUDIO	8 37	
TRUE	SYS_ONEWIRE	37 39	
TRUE	SMC_BC_ACOK	9 37 39 40	
TRUE	=USB_PWR_EN	36 37 58	
TRUE	SMC_LID	7 37 39 40 47	
TRUE	=I2C_LIO_SDA	37 42	
TRUE	=I2C_LIO_SCL	37 42	
TRUE	=I2C_MIKEY_SCL	37 42	
TRUE	=I2C_MIKEY_SDA	37 42	
TRUE	AUD_IPHS_SWITCH_EN	19 37	
TRUE	AUD_IP_PERIPHERAL_DET	17 37	
TRUE	AUD_I2C_INT_L	19 37	
TRUE	AUD_GPIO_3	37 49	
TRUE	SPKRAMP_INR_N	37 49 72	
TRUE	SPKRAMP_INR_P	37 49 72	
TRUE	USB_EXTD_N	18 37 69	
TRUE	USB_EXTD_P	18 37 69	
TRUE	USB_CAMERA_N	18 37 69	
TRUE	USB_CAMERA_P	18 37 69	
TRUE	HDA_SDOUT	19 37 69	
TRUE	HDA_BIT_CLK	19 37 69	
TRUE	HDA_SDIN0	19 37 69	
TRUE	USB_EXTD_OC_L	18 37	
TRUE	HDA_RST_L	19 37 69	
TRUE	HDA_SYNC	19 37 69	

(Need to add 5 GND TPs)

J4800: SD Card Connector

FUNC_TEST		
TRUE	PP3V3_SW_SD_PWR	38
TRUE	SD_CLK	38 70
TRUE	SD_CMD	38 70
TRUE	SD_D<7..0>	38 70
TRUE	SD_CD_L	38
TRUE	SD_WP	38

(Need to add 2 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST		
TRUE	=PP3V3_S5_LPCPLUS	8 41
TRUE	=PP5V_S0_LPCPLUS	8 41
TRUE	LPC_AD<3..0>	19 39 41 69
TRUE	SPI_ALT_MOSI	41 69
TRUE	SPI_ALT_MISO	41 69
TRUE	LPC_FRAME_L	19 39 41 69
TRUE	PM_CLKRUN_L	19 39 41
TRUE	SMC_TMS	39 40 41
TRUE	LPCPLUS_RESET_L	25 41
TRUE	SMC_TDO	39 40 41
TRUE	SMC_TRST_L	39 41
TRUE	SMC_MD1	39 41
TRUE	SMC_TX_L	36 39 40 41
TRUE	LPC_CLK33M_LPCPLUS	25 41 69
TRUE	SPIROM_USE_MLB	19 41 48
TRUE	SPI_ALT_CLK	41 69
TRUE	SPI_ALT_CS_L	41 69
TRUE	LPC_SERIRQ	19 39 41
TRUE	LPC_PWRDWN_L	19 39 41
TRUE	SMC_TDI	39 40 41
TRUE	SMC_TCK	39 40 41
TRUE	SMC_RESET_L	39 40 41 51
TRUE	SMC_NMI	39 41
TRUE	SMC_RX_L	36 39 40 41
TRUE	LPCPLUS_GPIO	19 41

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST		
TRUE	PP5V_S0	7 8 58
TRUE	FAN_RT_TACH	46
TRUE	FAN_RT_PWM	46

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST		
TRUE	=PP5V_S3_TPAD	8 57
TRUE	=PP3V42_G3H_TPAD	8 47
TRUE	=PP3V3_S3_TPAD	8 47
TRUE	USB_TPAD_CONN_P	47 72
TRUE	USB_TPAD_CONN_N	47 72
TRUE	=I2C_TPAD_SDA	42 47
TRUE	=I2C_TPAD_SCL	42 47
TRUE	SMC_ONOFF_L	39 40 47
TRUE	SMC_LID	7 37 39 40 47
TRUE	SMC_TPAD_RST_L	40 47

(Need to add 5 GND TPs)

J6900: DC-In Connector

FUNC_TEST			
TRUE	=PP18V5_DCIN_CONN	8 50	(Need 6 TPs)
TRUE	=PP5V_S3_LIO_CONN	8 50	

(Need to add 6 GND TPs)

J6903: Speaker Connector

FUNC_TEST		
TRUE	SPKRAMP_R_P_OUT	49 50
TRUE	SPKRAMP_R_N_OUT	49 50

J6950: Battery Connector

FUNC_TEST			
TRUE	PPVBAT_G3H_CONN	50 51	(Need 4 TPs)
TRUE	SMBUS_SMC_BSA_SCL	42 71	
TRUE	SMBUS_SMC_BSA_SDA	42 71	
TRUE	SYS_DETECT_L	50	

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST			
TRUE	PPVOUT_SW_LCDBKLT	7 43 60 63	(Need 2 TPs)
TRUE	PP3V3_SW_LCD	60	(Need 2 TPs)
TRUE	=I2C_TCON_SDA	42 60	
TRUE	LED_RETURN_6	60 63	
TRUE	LED_RETURN_5	60 63	
TRUE	LED_RETURN_4	60 63	
TRUE	LED_RETURN_3	60 63	
TRUE	LED_RETURN_2	60 63	
TRUE	LED_RETURN_1	60 63	
TRUE	DP_INT_HPD_CONN	60	
TRUE	DP_INT_AUX_CH_C_N	60 72	
TRUE	DP_INT_AUX_CH_C_P	60 72	
TRUE	DP_INT_ML_F_P<0>	60 72	
TRUE	DP_INT_ML_F_N<0>	60 72	
TRUE	DP_INT_ML_F_P<1>	60 72	
TRUE	DP_INT_ML_F_N<1>	60 72	
TRUE	=I2C_TCON_SCL	42 60	

(Need to add 5 GND TPs)

Misc Voltages & Control Signals

FUNC_TEST		
TRUE	PPVOUT_SW_LCDBKLT	7 43 60 63
TRUE	PPDCIN_S5_S5	8
TRUE	PPBUS_G3H	8 43 50
TRUE	PPBUS_G3H_ISNS	8
TRUE	PP5V_S3	8
TRUE	PP5V_S3_RTUSB_A_F	36
TRUE	PP5V_S0	7 8 58
TRUE	PP3V42_G3H	8
TRUE	PP3V3_S5	8 58 72
TRUE	PP3V3_SW_DPPWR	62
TRUE	PP3V3_S3	8
TRUE	PP3V3_WLAN_F	7 34 40
TRUE	PP3V3_S0	8 58 72
TRUE	PP3V3_S0_HDD_R	7 35
TRUE	PP3V3_ENET	8
TRUE	PP1V5R1V35_S3	8 72
TRUE	PP1V5_S0	8 58 72
TRUE	PP1V05_S0	8 58
TRUE	PP1V05_S0_MCP_PLL_UF	8
TRUE	PP0V9_S5	8
TRUE	PP0V9_ENET	8
TRUE	PPVCORE_S0_CPU	8 43
TRUE	PPVCORE_S0_MCP	8 43

(Need to add 27 GND TPs)

TRUE	SMC_PM_G2_EN	39 58
TRUE	PM_SLP_S4_L	19 39 58
TRUE	PM_SLP_S3_L	19 39 40 58

NO_TEST Nets

FSB Signals (Covered via CPU/MCP JTAG)

NO_TEST		
TRUE	FSB_A_L<35..3>	10 14 66
TRUE	FSB_ADS_L	10 14 66
TRUE	FSB_ADSTB_L<1..0>	10 14 66
TRUE	FSB_D_L<63..0>	10 14 66
TRUE	FSB_DINV_L<3..0>	10 14 66
TRUE	FSB_DSTB_L_N<3..0>	10 14 66
TRUE	FSB_DSTB_L_P<3..0>	10 14 66
TRUE	FSB_HIT_L	10 14 66
TRUE	FSB_HITM_L	10 14 66
TRUE	FSB_LOCK_L	10 14 66
TRUE	FSB_REQ_L<4..0>	10 14 66

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/16/2010)

PAGE TITLE
Functional Test / No Test

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

PAGE 7 OF 110

SHEET 7 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

"G3Hot" (Always-Present) Rails

=PP18V5_DCIN_CONN — PPDCIN_S5_S5
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR

=PPBUS_G3H — PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.4V
MAKE_BASE=TRUE
=PPBUS_G3H_R_IN
=PPBUS_S0_LCDBKLT
=PPVIN_S5_P5VP3V3
=PPBUS_5V_S5

=PPBUS_G3H_R_OUT — PPBUS_G3H_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=8.4V
MAKE_BASE=TRUE
=PPVIN_S5_CPU_IMVP
=PPVIN_S3_DDRREG
=PPVIN_S0_MCPCORE
=PPVIN_S0_CPUVTTS0

=PP3V42_G3H_REG — PP3V42_G3H
0.064
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
PP3V3_G3_RTC
=PP3V42_G3H_SMCUSBMUX
=PP3V42_G3H_ONEWIRE
=PP3V42_G3H_SMBUS_SMC_BSA
=PP3V42_G3H_BMON_ISNS
=PP3V42_G3H_TPAD
=PP3V42_G3H_CHGR
=PP3V42_G3H_PWRCTL
=PP3V3_S5_SMC
=PP3V3_S5_LPCPLUS
=PPVIN_S5_SMCVREF

"S5" Rails

=PP3V3_S5_REG — PP3V3_S5
1.07 A + S3 + S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_MCP_GPIO
=PP3V3_S5_MCP
=PP3V3_S5_MCPPWRGD
=PP3V3_S5_SMBUS_SMC_MGMT
=PP3V3_S5_ROM
=PP3V3_S5_P0V9S5
=PP3V3_S5_VMON
=PP3V3_S5_P3V3S3FET
=PP3V3_S5_P3V3ENETFET
=PP3V3_S5_P3V3S0FET
=PP3V3_S5_P0V9ENETFET
=PP3V3_S5_DP_PORT_PWR
=PP3V3_S0_LCD
=PP3V3_S5_TPAD
=PP3V3_SMC_PME

=PP0V9_S5_REG — PP0V9_S5
0.290 A
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
105 mA/241 mA =PP0V9_S5_MCP_VDD_AUXC
=PP0V9_ENET_P0V9ENETFET

"S3" Rails

=PP3V3_S3_FET — PP3V3_S3
1.274 A
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_MCP_GPIO
=PP3V3_S3_VREFMRGN
=PP3V3_S3_BT
=PP3V3_S3_WLAN
=PP3V3_S3_CARDREADER
=PP3V3_S3_SMBUS_SMC_A_S3
=PP3V3_S3_1V5S3ISNS
=PP3V3_S3_WLANISNS
=PP3V3_S3_TPAD
=PP3V3_S3_SMS
=PP3V3_S3_DBGLEDS
=PP3V3_S3_PDCISENS

=PP5V_S3_REG — PP5V_S3
5.40 A
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_MCPDDRFET
=PP5V_S3_RTUSB
=PP5V_S3_SYSLED
=PP5V_S3_TPAD
=PP5V_S3_AUDIO_AMP
=PP5V_S3_LIO_CONN
=PP5V_S3_DDRREG
=PP5V_S3_P5VS0FET

=PPDDR_S3_REG — PP1V5R1V35_S3
11.30 A
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE (OR 1.35V)
=PP1V5R1V35_S3_MCP_MEM
=PP1V5R1V35_S0_MCPDDRFET
0 mA =PPLVDDR_S3_MEM_A
4250 mA =PPLVDDR_S3_MEM_B
=PPVIN_S0_DDRREG_LDO

=PPVTT_S3_DDR_BUF — PPDDRVREF_S3
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE (OR 0.675V)

"ENET" Rails

=PP3V3_ENET_FET_R — PP3V3_ENET
300mA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
300mA =PP3V3_ENET_MCP_RMGT
=PP3V3_ENET_MCP_PLL_MAC

=PP0V9_ENET_FET — PP0V9_ENET
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V9_ENET_MCP_RMGT

"S0" Rails

=PP5V_S0_FET — PP5V_S0
0.100 A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_MCPFSBFET
=PP5V_S0_LPCPLUS
=PP5V_S0_FAN
=PP5V_S0_CPU_IMVP
=PP5V_S0_MCPREG
=PP5V_S0_CPUVTTS0
=PP5V_S0_BKL
=PP5VR3V3_S0_DPCADET

=PP3V3_S0_FET — PP3V3_S0
3.30 A
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_XDP
=PP3V3_S0_MCP_GPIO
=PP3V3_S0_MCP_HVDD
=PP3V3_S0_MCP
=PP3V3_S0_MCP_PLL_UF
=PP3V3_S0_HDD
=PP3V3_S0_AUDIO
=PP3V3_S0_SMC
=PP3V3_S0_DEBUGROM
=PP3V3_S0_SMBUS_MCP_0
=PP3V3_S0_SMBUS_MCP_1
=PP3V3_S0_SMBUS_SMC_B_S0
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_BKLTISNS
=PP3V3_S0_HDDISNS
=PP3V3_S0_CSREGISNS
=PP3V3_S0_MCPCOREISNS
=PP3V3_S0_MCPDDRISNS
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_MCPTHMSNS
=PP3V3_S0_FAN
=PP3V3_S0_IMVP
=PP3V3_S0_MCP_PLL_VLDO
=PP3V3_S0_P1V5S0
=PP3V3_S0_PWRCTL
=PP3V3_S0_DPCONN
=PP3V3_S0_BKL_VDDIO

=PP1V5_S0_REG — PP1V5_S0
0.210 A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU
=PP1V5_S0_MCP_PLL_VLDO
=PP3V3R1V5_S0_MCP_HDA
=PP1V8R1V5_S0_AUDIO

=PPCPUVTT_S0_REG — PP1V05_S0
9.40 A
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU
=PP1V05_S0_XDP
=PP1V05_S0_MCP_FSB
=PP1V05_S0_MCP_M2CLK_DLL
=PP1V05_S0_MCP_DP0_VDD
=PP1V05_S0_MCP_PE_DVDD
=PP1V05_S0_MCP_SATA_DVDD
=PP1V05_S0_MCP_AVDD_UF
=PP1V05_S0_MCP_PLL_UF_R
=PP1V05_SW_MCP_FSB

=PP1V05_S0_MCP_PLL_OR — PP1V05_S0_MCP_PLL_UF
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PLL_UF

=PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU
18 A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU

=PPMCPCORE_S0_REG — PPVCORE_S0_MCP
23.8 A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP
=PPVCORE_S0_MCPGFXFET

=PPVTT_S0_DDR_LDO — PPDDRVTT_S0
1.20 A
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE (OR 0.675V)
=PPDDRVTT_S0_MEM_A
=PPDDRVTT_S0_MEM_B

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/11/2010)

PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 8 OF 110
SHEET 8 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Plated Board Slot

SL0900
TH-NSP
SL-2.3X3.9-2.9X4.5

CPU Heat Sink Mounting Bosses

Z0913 STDOFF-4.5OD1.8H-SM
Z0910 STDOFF-4.5OD1.8H-SM
Z0911 STDOFF-4.5OD1.8H-SM
Z0912 STDOFF-4.5OD1.8H-SM
4x 860-1327

MCP Heat Sink Mounting Bosses

Z0906 STDOFF-4.5OD1.8H-SM
Z0909 STDOFF-4.5OD1.8H-SM
Z0908 STDOFF-4.5OD1.8H-SM
Z0907 STDOFF-4.5OD1.8H-SM
4x 860-1327

Fan Boss

Z0905
STDOFF-4.5OD1.8H-SM
860-1327

X21 Boss

Z0914
STDOFF-4.5OD1.9H-SM
860-1327

SSD Boss

Z0915
STDOFF-4.5OD1.9H-SM
860-1327

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL
ZS0905
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

USB/SD Card Pogo

CRITICAL
ZS0906
POGO-2.0OD-3.6H-K86-K87
SM
870-1938

DisplayPort PCB Stiffener

(Provides PCB support for small finger above J9400)

NO STUFF
MT0900
STIFFENER-K16-K99
SM-SP
806-1176

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.1 mm
MIN_LINE_WIDTH=0.5 mm

CPU Aliases

66 10 IN	CPU_BSEL<0:2>	=MCP_BSEL<0:2>	OUT 14
14 BI	CPU_PECI_MCP	TP_CPU_PECI_MCP	

DisplayPort Aliases

External DisplayPort Signals

68 17 IN	DP_IG_ML0_P<0..3>	DP_EXT_ML_P<0..3>	OUT 62 72
68 17 IN	DP_IG_ML0_N<0..3>	DP_EXT_ML_N<0..3>	OUT 62 72
68 17 BI	DP_IG_AUX_CH0_P	DP_EXT_AUX_CH_P	BI 61
68 17 BI	DP_IG_AUX_CH0_N	DP_EXT_AUX_CH_N	BI 61
17 OUT	DP_IG_HPD0	DP_EXT_HPD	IN 62
61 OUT	DP_CA_DET	DP_EXT_CA_DET	IN 62
61 BI	DP_AUX_CH_C_N	DP_EXT_AUX_CH_C_N	BI 62 72
61 BI	DP_AUX_CH_C_P	DP_EXT_AUX_CH_C_P	BI 62 72

Internal DisplayPort Signals

68 17 IN	DP_IG_ML1_P<0..1>	DP_INT_ML_P<0..1>	OUT 60 72
68 17 IN	DP_IG_ML1_N<0..1>	DP_INT_ML_N<0..1>	OUT 60 72
68 17 BI	DP_IG_AUX_CH1_P	DP_INT_AUX_CH_P	BI 60 72
68 17 BI	DP_IG_AUX_CH1_N	DP_INT_AUX_CH_N	BI 60 72
17 OUT	DP_IG_HPD1	DP_INT_HPD	IN 60
17 IN	DP_IG_ML1_P<2..3>	TP_DP_INT_MLP<2..3>	
17 IN	DP_IG_ML1_N<2..3>	TP_DP_INT_MLN<2..3>	
17 IN	LCD_IG_BKLT_PWM	LCD_BKLT_PWM	OUT 63
60 17 9 IN	LCD_IG_PWR_EN	LCD_IG_PWR_EN	OUT 9 17 60
17 IN	LCD_IG_BKLT_EN	LCD_BKLT_EN	OUT 64

Ethernet Aliases

16 OUT	ENET_CLKREQ_L	NC_ENET_CLKREQ_L (MAKE_BASE=TRUE NO_TEST=TRUE)	

R0911
0
5%
1/16W
MF
402

PP3V3_ENET_FET (MIN_LINE_WIDTH=0.2 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.47V, MAKE_BASE=TRUE) — =PP3V3_ENET_FET (59) — 1 — 2 — =PP3V3_ENET_FET_R (PLACE_NEAR=U7980.A1:5MM) OUT 8

ENET_RXD_PD (MAKE_BASE=TRUE)	ENET_RXD<0>	OUT 18 70
	ENET_RXD<1>	OUT 18 70
	ENET_RXD<2>	OUT 18 70
	ENET_RXD<3>	OUT 18 70
ENET_RXCLK_PD (MAKE_BASE=TRUE)	ENET_CLK125M_RXCLK	OUT 18 70
	ENET_RX_CTRL	OUT 18 70
	ENET_MDIO	BI 18 70
	MCP_RGMII_VREF	OUT 18
	ENET_ENERGY_DET	OUT 18

R0980[1] 10K 5% 1/20W MF 201 2
R0981[1] 10K 5% 1/20W MF 201 2
R0984[1] 10K 5% 1/20W MF 201 2
R0982[1] 10K 5% 1/20W MF 201 2
R0983[1] 10K 5% 1/20W MF 201 2
R0985[1] 10K 5% 1/20W MF 201 2

Charger Signal

51 IN	=CHGR_ACOK	SMC_BC_ACOK (MAKE_BASE=TRUE)	OUT 7 37 39 40

MCPCOREISNS Signals

55 IN	MCPCORES0_VO (MAKE_BASE=TRUE)	=MCPCOREISNS_N	OUT 44
55 IN	MCPCORES0_ISP_R (MAKE_BASE=TRUE)	=MCPCOREISNS_P	OUT 44

LVDS Aliases

17 IN	=MCP_IFPA_TXC_P	NC_LVDS_IG_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE)
17 IN	=MCP_IFPA_TXC_N	NC_LVDS_IG_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE)
17 IN	=MCP_IFPA_TXD_P<0..3>	NC_LVDS_IG_A_DATAP<0..3> (MAKE_BASE=TRUE NO_TEST=TRUE)
17 IN	=MCP_IFPA_TXD_N<0..3>	NC_LVDS_IG_A_DATAN<0..3> (MAKE_BASE=TRUE NO_TEST=TRUE)
17 IN	=MCP_IFPB_TXC_P	NC_LVDS_IG_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE)
17 IN	=MCP_IFPB_TXC_N	NC_LVDS_IG_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE)
17 IN	=MCP_IFPB_TXD_P<0..3>	NC_LVDS_IG_B_DATAP<0..3> (MAKE_BASE=TRUE NO_TEST=TRUE)
17 IN	=MCP_IFPB_TXD_N<0..3>	NC_LVDS_IG_B_DATAN<0..3> (MAKE_BASE=TRUE NO_TEST=TRUE)
17 IN	=MCP_IFPAB_DDC_CLK	TP_LVDS_DDC_CLK (MAKE_BASE=TRUE)
17 BI	=MCP_IFPAB_DDC_DATA	TP_LVDS_DDC_DATA (MAKE_BASE=TRUE)

PCI-E Aliases

Unused PCI-E Lanes

16 IN	=PEG_R2D_C_N<5:4>	NC_PEG_R2DCN<5:4> (MAKE_BASE=TRUE NO_TEST=TRUE)
16 IN	=PEG_R2D_C_P<5:4>	NC_PEG_R2DCP<5:4> (MAKE_BASE=TRUE NO_TEST=TRUE)
16 OUT	=PEG_D2R_N<5:4>	NC_PEG_D2RN<5:4> (MAKE_BASE=TRUE NO_TEST=TRUE)
16 OUT	=PEG_D2R_P<5:4>	NC_PEG_D2RP<5:4> (MAKE_BASE=TRUE NO_TEST=TRUE)
68 16 IN	PEG_CLK100M_P	NC_PEG_CLK100MP (MAKE_BASE=TRUE NO_TEST=TRUE)
68 16 IN	PEG_CLK100M_N	NC_PEG_CLK100MN (MAKE_BASE=TRUE NO_TEST=TRUE)
16 OUT	PEG_CLKREQ_L	NC_PEG_CLKREQ_L (MAKE_BASE=TRUE NO_TEST=TRUE)

SATA Aliases

Unused SATA ODD Signals

68 18 IN	SATA_ODD_R2D_C_P	NC_SATA_ODD_R2DCP (MAKE_BASE=TRUE NO_TEST=TRUE)
68 18 IN	SATA_ODD_R2D_C_N	NC_SATA_ODD_R2DCN (MAKE_BASE=TRUE NO_TEST=TRUE)
68 18 OUT	SATA_ODD_D2R_P	NC_SATA_ODD_D2RP (MAKE_BASE=TRUE NO_TEST=TRUE)
68 18 OUT	SATA_ODD_D2R_N	NC_SATA_ODD_D2RN (MAKE_BASE=TRUE NO_TEST=TRUE)

USB Aliases

Unused USB Ports

69 18 BI	USB_MINI_P	NC_USB_MINIP (MAKE_BASE=TRUE NO_TEST=TRUE)
69 18 BI	USB_MINI_N	NC_USB_MININ (MAKE_BASE=TRUE NO_TEST=TRUE)
69 18 BI	USB_EXTC_P	NC_USB_EXTCP (MAKE_BASE=TRUE NO_TEST=TRUE)
69 18 BI	USB_EXTC_N	NC_USB_EXTCN (MAKE_BASE=TRUE NO_TEST=TRUE)

Misc MCP89 Aliases

17	TP_MCP_RGB_DAC_VREF	NC_MCP_RGB_DAC_VREF (MAKE_BASE=TRUE NO_TEST=TRUE)
67 15 IN	MEM_A_CLK_P<1>	TP_MEM_A_CLKP<1> (MAKE_BASE=TRUE)
67 15 IN	MEM_A_CLK_N<1>	TP_MEM_A_CLKN<1> (MAKE_BASE=TRUE)
67 15 IN	MEM_B_CLK_P<1>	TP_MEM_B_CLKP<1> (MAKE_BASE=TRUE)
67 15 IN	MEM_B_CLK_N<1>	TP_MEM_B_CLKN<1> (MAKE_BASE=TRUE)
67 15 IN	MEM_A_A<15>	TP_MEM_A_A<15> (MAKE_BASE=TRUE)
67 15 IN	MEM_B_A<15>	TP_MEM_B_A<15> (MAKE_BASE=TRUE)
19 IN	MCP_MEM_VDD_SEL_1V5	TP_MEM_VDD_SEL_1V5 (MAKE_BASE=TRUE)

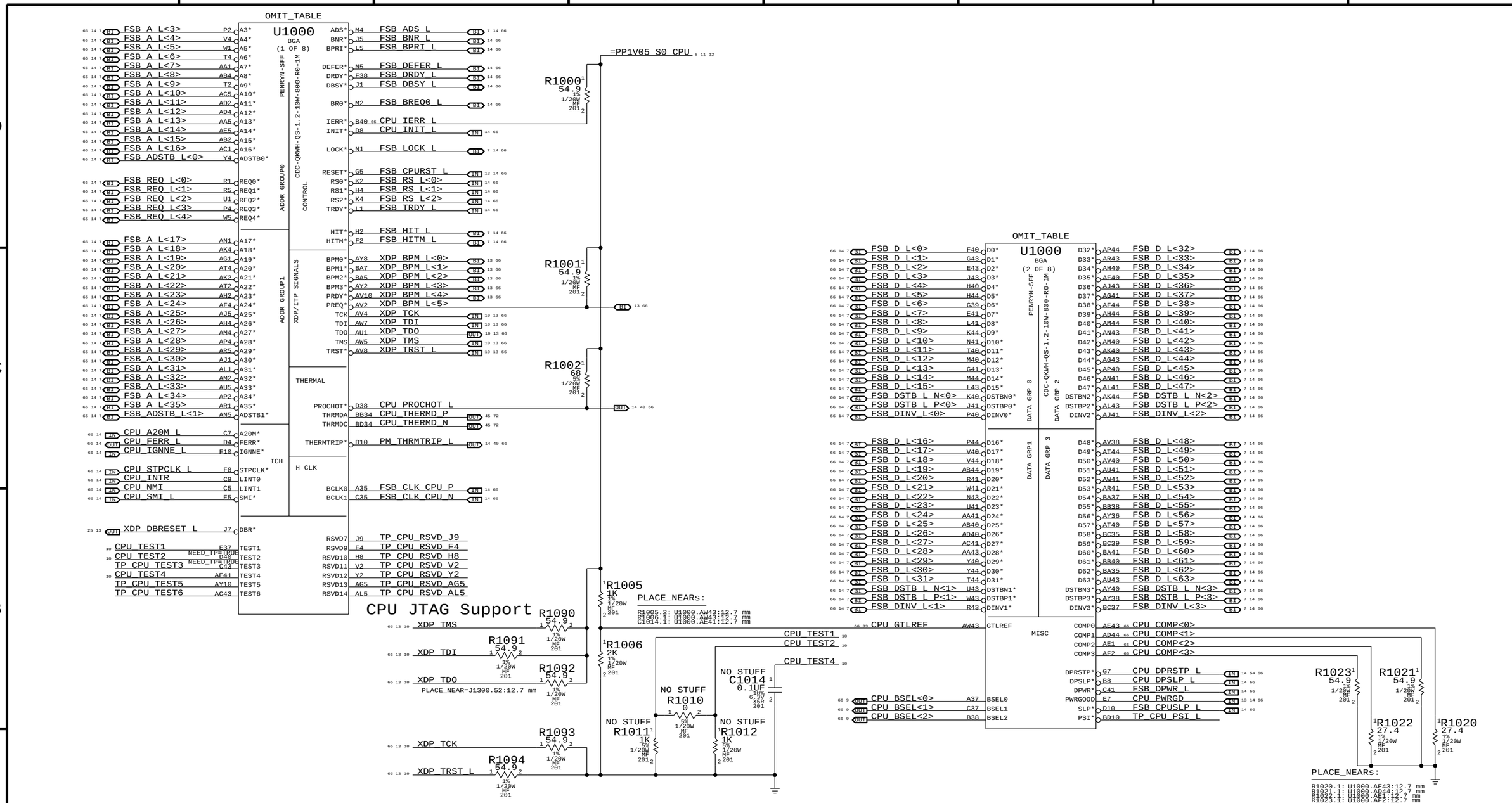
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE
Signal Aliases

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 9 OF 110
SHEET 9 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE

CPU FSB

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

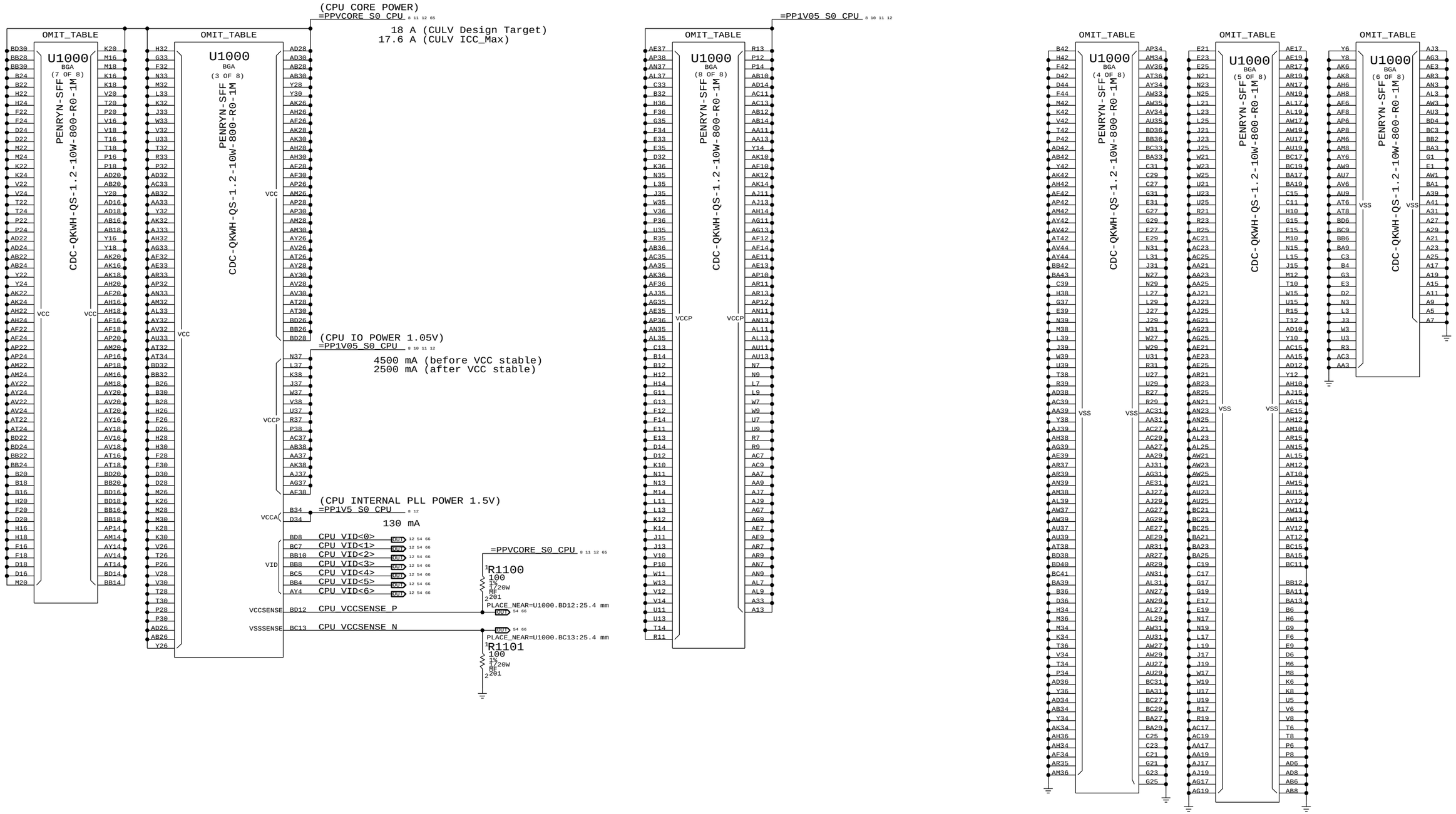
BRANCH

PAGE 10 OF 110

SHEET 10 OF 74

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

PAGE TITLE
CPU Power & Ground

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

PAGE 11 OF 110

SHEET 11 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CPU VCORE HF AND BULK DECOUPLING

4x 270uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

65 11 8 =PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL NO STUFF C1200 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1201 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1202 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1203 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1204 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1205 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1206 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1207 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1208 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1209 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1210 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1211 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1212 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1213 10UF 20% 6.3V X5R 603	CRITICAL OMIT_TABLE C1214 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1215 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1216 10UF 20% 6.3V X5R 603	CRITICAL OMIT_TABLE C1217 10UF 20% 6.3V X5R 603	CRITICAL OMIT_TABLE C1218 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1219 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL NO STUFF C1220 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1221 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1222 10UF 20% 6.3V X5R 603	CRITICAL OMIT_TABLE C1223 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1224 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1225 10UF 20% 6.3V X5R 603	CRITICAL OMIT_TABLE C1226 10UF 20% 6.3V X5R 603	CRITICAL OMIT_TABLE C1227 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1228 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1229 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1230 10UF 20% 6.3V X5R 603	CRITICAL NO STUFF C1231 10UF 20% 6.3V X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1240 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1241 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1242 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1243 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1244 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1245 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1246 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1247 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1248 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1249 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1250 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1251 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1252 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1253 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1254 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1255 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1256 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1257 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1258 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1259 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL OMIT_TABLE C1260 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1261 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1262 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1263 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1264 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1265 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1266 2.2UF 20% 6.3V CERM 402-LF	CRITICAL OMIT_TABLE C1267 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

CRITICAL C1270 270UF 20% 2V TANT CASE-B4-SM	CRITICAL C1271 270UF 20% 2V TANT CASE-B4-SM	CRITICAL C1272 270UF 20% 2V TANT CASE-B4-SM	CRITICAL C1273 270UF 20% 2V TANT CASE-B4-SM

CPU VCORE VID CONNECTIONS

66 54 11 IN CPU_VID<0..6> MAKE_BASE=TRUE — IMVP6_VID<0..6> OUT 66

VCCA (CPU AVdd) DECOUPLING

11 8 =PP1V5_S0_CPU 1x 10uF, 1x 0.01uF

OMIT_TABLE C1280 10uF 20% 6.3V X5R 603

C1281 0.01UF 10% 10V X5R 201

LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

VCCP (CPU I/O) DECOUPLING

11 10 8 =PP1V05_S0_CPU 1x 270uF, 12x 2.2uF

OMIT_TABLE C1283 2.2UF 20% 6.3V CERM 402-LF	OMIT_TABLE C1284 2.2UF 20% 6.3V CERM 402-LF	OMIT_TABLE C1285 2.2UF 20% 6.3V CERM 402-LF	OMIT_TABLE C1286 2.2UF 20% 6.3V CERM 402-LF	OMIT_TABLE C1287 2.2UF 20% 6.3V CERM 402-LF	OMIT_TABLE C1288 2.2UF 20% 6.3V CERM 402-LF

CRITICAL C1290 270UF 20% 2V TANT CASE-B4-SM

OMIT_TABLE C1291 2.2UF 20% 6.3V CERM 402-LF	OMIT_TABLE C1292 2.2UF 20% 6.3V CERM 402-LF	OMIT_TABLE C1293 2.2UF 20% 6.3V CERM 402-LF	OMIT_TABLE C1294 2.2UF 20% 6.3V CERM 402-LF	OMIT_TABLE C1295 2.2UF 20% 6.3V CERM 402-LF	OMIT_TABLE C1296 2.2UF 20% 6.3V CERM 402-LF

LAYOUT NOTE:
PLACE C1290 CLOSE TO CPU
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/11/2010)

PAGE TITLE
CPU Decoupling & VID

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

PAGE 12 OF 110

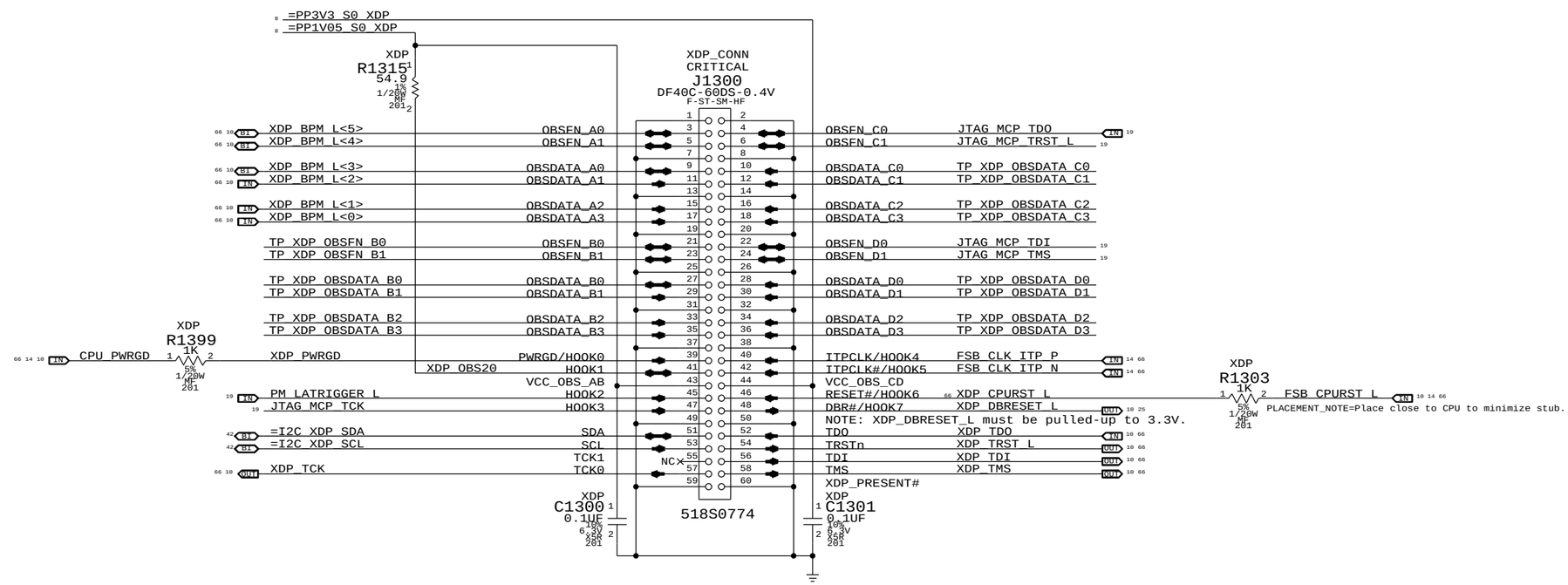
SHEET 12 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Micro2-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0782 Adapter Flex to support chipset debug.



Direction of XDP adapter flex

Please place J1300 within 1" of board edge with odd-numbered pins facing edge. Avoid any tall components between J1300 and edge.

SYNC_MASTER=K99_MLB SYNC_DATE=03/01/2010

PAGE TITLE: eXtended Debug Port (Micro-XDP)

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

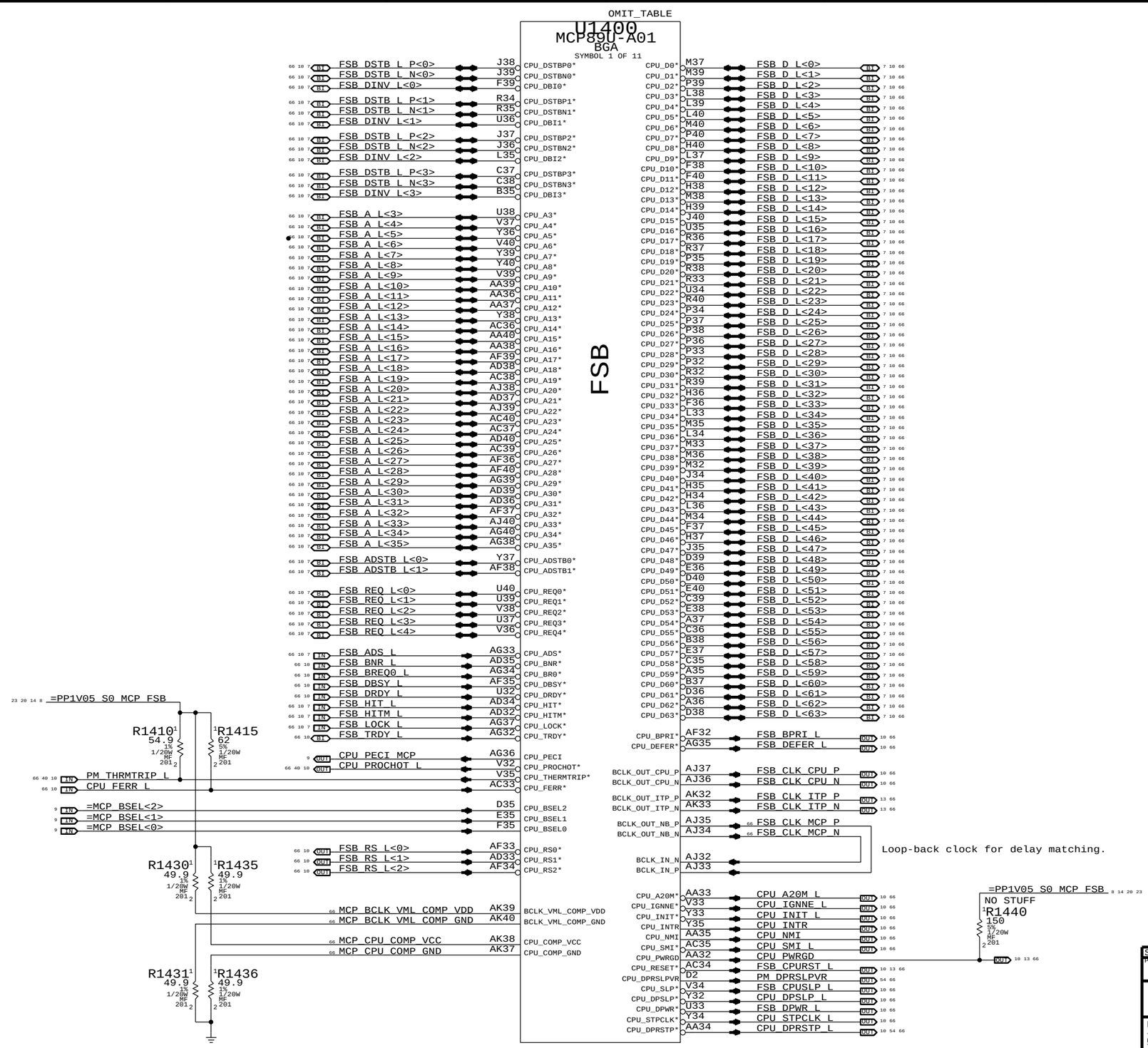
REVISION: 3.3.0

BRANCH:

PAGE: 13 OF 110

SHEET: 13 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE

MCP CPU Interface

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

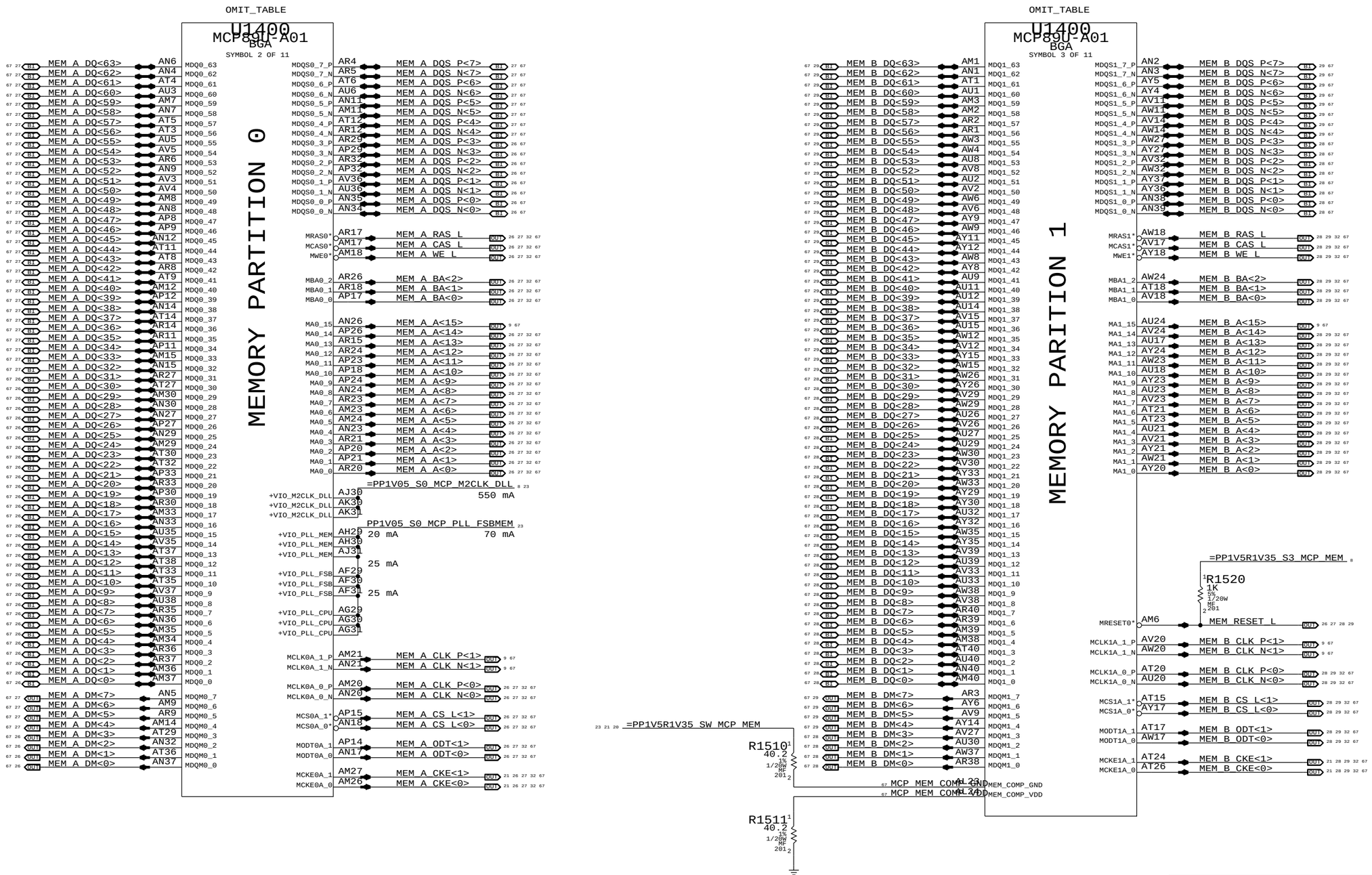
REVISION 3.3.0

BRANCH

PAGE 14 OF 110

SHEET 14 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
MCP Memory Interface

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

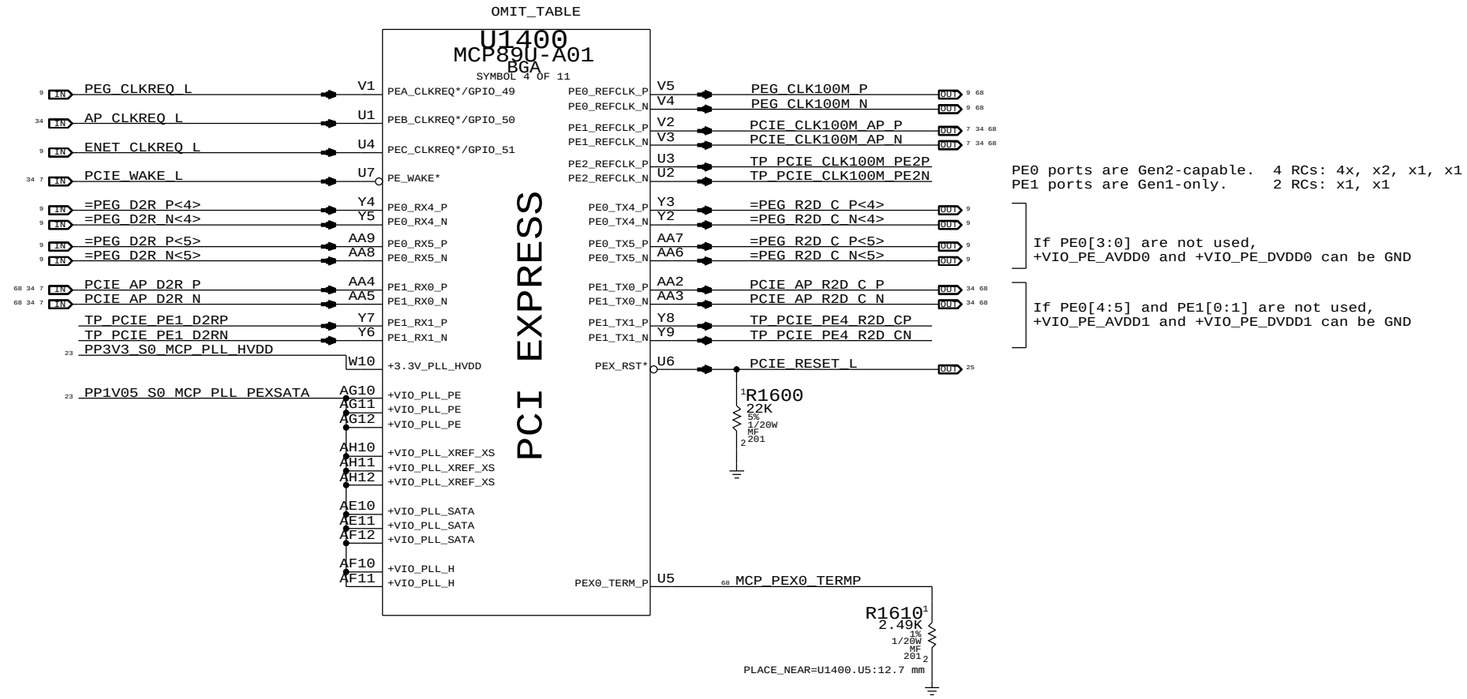
REVISION 3.3.0

BRANCH

PAGE 15 OF 110

SHEET 15 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1
PE1 ports are Gen1-only. 2 RCs: x1, x1

If PE0[3:0] are not used,
+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

If PE0[4:5] and PE1[0:1] are not used,
+VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 16 OF 110
SHEET 16 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT_TABLE

U1400
MCP89U-A01
BGA
SYMBOL 5 OF 11

RGB

Pin	Signal	Net
K30	+3.3V_RGBDAC	PP3V3_S0_MCP_DAC, 140 mA
J29	RGB_DAC_VREF	TP_MCP_RGB_DAC_VREF
G30	DDC_CLK0/GPIO_38	AUD_IP_PERIPHERAL_DET
F30	DDC_DATA0/GPIO_39	MIKEY_MIC_LOAD_DET

FLAT PANEL

Pin	Signal	Net
H27	DP0_3_P/TMDS0_TXC_P	DP_IG_ML0_P<3>
J27	DP0_3_N/TMDS0_TXC_N	DP_IG_ML0_N<3>
D26	DP0_2_P/TMDS0_TX0_P	DP_IG_ML0_P<2>
C26	DP0_2_N/TMDS0_TX0_N	DP_IG_ML0_N<2>
F26	DP0_1_P/TMDS0_TX1_P	DP_IG_ML0_P<1>
E26	DP0_1_N/TMDS0_TX1_N	DP_IG_ML0_N<1>
H26	DP0_0_P/TMDS0_TX2_P	DP_IG_ML0_P<0>
G26	DP0_0_N/TMDS0_TX2_N	DP_IG_ML0_N<0>
F27	DP1_3_P/TMDS0B_TXC_P	DP_IG_ML1_P<3>
G27	DP1_3_N/TMDS0B_TXC_N	DP_IG_ML1_N<3>
E27	DP1_2_P/TMDS0_TX3_P	DP_IG_ML1_P<2>
D27	DP1_2_N/TMDS0_TX3_N	DP_IG_ML1_N<2>
C27	DP1_1_P/TMDS0_TX4_P	DP_IG_ML1_P<1>
B27	DP1_1_N/TMDS0_TX4_N	DP_IG_ML1_N<1>
A29	DP1_0_P/TMDS0_TX5_P	DP_IG_ML1_P<0>
B29	DP1_0_N/TMDS0_TX5_N	DP_IG_ML1_N<0>
C29	HPLUG_DET0/GPIO_20	DP_IG_HPD0
D30	HPLUG_DET1/GPIO_21	DP_IG_HPD1
E30	HPLUG_DET2/GPIO_22	SATARDRVR_A_EN
E29	DDC_CLK2/DP_AUX_CH0_P	DP_IG_AUX_CH0_P
D29	DDC_DATA2/DP_AUX_CH0_N	DP_IG_AUX_CH0_N
G29	DDC_CLK3/DP_AUX_CH1_P	DP_IG_AUX_CH1_P
F29	DDC_DATA3/DP_AUX_CH1_N	DP_IG_AUX_CH1_N
L23	+3.3V_PLL_DP0	PP3V3_S0_MCP_PLL_DP_USB, 210 mA, 180 mA
M23	+3.3V_PLL_DP0	
L22	+3.3V_PLL_USB	30 mA
M22	+3.3V_PLL_USB	
L25	+VIO_PLL_IFPAB	=PP1V05_S0_MCP_PLL_IFP, 60 mA
M25	+VIO_PLL_IFPAB	
L26	+VIO_PLL_CORE_LEG	PP1V05_S0_MCP_PLL_CORE, 160 mA, 40 mA
M26	+VIO_PLL_CORE_LEG	
L27	+VIO_PLL_SPPLL0	60 mA
M27	+VIO_PLL_SPPLL0	
L28	+VIO_PLL_V	40 mA
M28	+VIO_PLL_V	
L24	+VIO_PLL_NV	20 mA
M24	+VIO_PLL_NV	
A23	+VDD_IFPA	=PP3V3R1V8_S0_MCP_IFP_VDD, 180 mA, CKPLUS_WAIVE=PwrTerm2Gnd
A24	+VDD_IFPB	CKPLUS_WAIVE=PwrTerm2Gnd
B26	+VIO_DP0	=PP1V05_S0_MCP_DP0_VDD, 160 mA
A27	+VIO_DP0	
A26	+VIO_DP0	
K24	IFPA_TXC_P	=MCP_IFPA_TXC_P
K23	IFPA_TXC_N	=MCP_IFPA_TXC_N
B23	IFPA_TXD0_P	=MCP_IFPA_TXD_P<0>
C23	IFPA_TXD0_N	=MCP_IFPA_TXD_N<0>
D23	IFPA_TXD1_P	=MCP_IFPA_TXD_P<1>
E23	IFPA_TXD1_N	=MCP_IFPA_TXD_N<1>
F23	IFPA_TXD2_P	=MCP_IFPA_TXD_P<2>
G23	IFPA_TXD2_N	=MCP_IFPA_TXD_N<2>
H23	IFPA_TXD3_P	=MCP_IFPA_TXD_P<3>
J23	IFPA_TXD3_N	=MCP_IFPA_TXD_N<3>
J24	IFPB_TXC_P	=MCP_IFPB_TXC_P
H24	IFPB_TXC_N	=MCP_IFPB_TXC_N
G24	IFPB_TXD4_P	=MCP_IFPB_TXD_P<0>
F24	IFPB_TXD4_N	=MCP_IFPB_TXD_N<0>
E24	IFPB_TXD5_P	=MCP_IFPB_TXD_P<1>
D24	IFPB_TXD5_N	=MCP_IFPB_TXD_N<1>
C24	IFPB_TXD6_P	=MCP_IFPB_TXD_P<2>
B24	IFPB_TXD6_N	=MCP_IFPB_TXD_N<2>
J26	IFPB_TXD7_P	=MCP_IFPB_TXD_P<3>
K26	IFPB_TXD7_N	=MCP_IFPB_TXD_N<3>
J30	DDC_CLK1/GPIO_40	=MCP_IFPAB_DDC_CLK
H30	DDC_DATA1/GPIO_41	=MCP_IFPAB_DDC_DATA
B30	LCD_BKL_CTL/GPIO_57	(GMUX_INT) LCD_IG_BKLT_PWM
C30	LCD_BKL_ON/GPIO_59	LCD_IG_BKLT_EN
A30	LCD_PANEL_PWR/GPIO_58	LCD_IG_PWR_EN
C21	IFPAB_VPROBE	MCP_IFPAB_VPROBE
B21	IFPAB_RSET	MCP_IFPAB_RSET
H29	TMDS0_VPROBE	MCP_TMDS0_VPROBE
K27	TMDS0_RSET	MCP_TMDS0_RSET

NOTE: 100K pull-downs required if HPLUG_DET0/HPLUG_DET1 are not used.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
Connect +3.3V_RGBDAC pin to GND.

NOTE: No Composite/S-Video/Component Video support on MCP89

Interface Mode

MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD_IFPx at 1.8V
TMDS: Power +VDD_IFPx at 3.3V

DDC Mode Pull-downs

NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.

R1710	100K	5%	1/20W	MF	201	DP_IG_AUX_CH0_P
R1711	100K	5%	1/20W	MF	201	DP_IG_AUX_CH0_N
R1712	100K	5%	1/20W	MF	201	DP_IG_AUX_CH1_P
R1713	100K	5%	1/20W	MF	201	DP_IG_AUX_CH1_N

GPIO Pull-Ups

=PP3V3_S0_MCP_GPIO

R1780	10K	5%	1/20W	MF	201	SATARDRVR_A_EN
R1781	10K	5%	1/20W	MF	201	AUD_IP_PERIPHERAL_DET
R1782	10K	5%	1/20W	MF	201	MIKEY_MIC_LOAD_DET

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
MCP Graphics

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 17 OF 110
SHEET 17 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT_TABLE

U1400
MCP89U-A01
BGA
SYMBOL 6 OF 11

SATA

SATA_HDD_R2D_C_P	AF1	SATA_A0_TX_P
SATA_HDD_R2D_C_N	AG1	SATA_A0_TX_N
SATA_HDD_D2R_N	AG3	SATA_A0_RX_N
SATA_HDD_D2R_P	AG2	SATA_A0_RX_P
SATA_ODD_R2D_C_P	AF2	SATA_A1_TX_P
SATA_ODD_R2D_C_N	AF3	SATA_A1_TX_N
SATA_ODD_D2R_N	AF5	SATA_A1_RX_N
SATA_ODD_D2R_P	AF4	SATA_A1_RX_P
MXM_GOOD_L	AG5	SATA_LED*/GPIO_30
MCP_SATA_TERMP	AG4	SATA_TERMP

=PP3V3_S0_MCP_GPIO — R1800 100K 5% 1/20W MF 201

R1805 2.49K 1% 1/20W MF 201

NC: G5, V6, AM4, H15, AK36

USB

OHCI0/EHCI0 — Internal 19.5K Pull-Downs on all USB pairs

OHCI1/EHCI1 — Only USB8-11 support nV USB JTAG in S3/S4/S5.

External A		
USB0_P	E21	USB_EXTA_P
USB0_N	D21	USB_EXTA_N
AirPort (PCIe Mini-Card)		
USB1_P	F21	USB_MINI_P
USB1_N	G21	USB_MINI_N
Geyser Trackpad/Keyboard		
USB2_P	E20	USB_TPAD_P
USB2_N	D20	USB_TPAD_N
External C		
USB3_P	L21	USB_EXTC_P
USB3_N	K21	USB_EXTC_N
Bluetooth		
USB4_P	A20	USB_BT_P
USB4_N	A21	USB_BT_N
Camera/External E		
USB5_P	H21	USB_CAMERA_P
USB5_N	J21	USB_CAMERA_N
SD Card/ExpressCard		
USB6_P	G20	USB_SDCARD_P
USB6_N	F20	USB_SDCARD_N
EXTERNAL D		
USB7_P	H20	USB_EXTD_P
USB7_N	J20	USB_EXTD_N
USB_OC0*/GPIO_25	H14	USB_EXTA_OC_L
USB_OC1*/GPIO_26	G12	USB_EXTD_OC_L
USB_RBIAS_GND	L19	MCP_USB_RBIAS_GND

=PP3V3_S5_MCP_GPIO — R1851 8.2K 5% 1/20W MF 201 — R1850 8.2K 5% 1/20W MF 201

R1860 887 1% 1/20W MF 201

LAN

ENET_RXD<0>	C15	RGMII_RXD0
ENET_RXD<1>	H17	RGMII_RXD1
ENET_RXD<2>	C17	RGMII_RXD2
ENET_RXD<3>	G15	RGMII_RXD3
ENET_CLK125M_RXCLK	D17	RGMII_RXCLK
ENET_RX_CTRL	A15	RGMII_RXCTL
ENET_ENERGY_DET	E17	RGMII_INTR/GPIO_35
PP3V3_ENET_MCP_PLL_MAC 20 mA	J18	+3.3V_PLL_MAC_DUAL
MCP_MII_COMP_VDD	K15	RGMII_COMP_VDD
MCP_MII_COMP_GND	K14	RGMII_COMP_GND
RGMII_VREF	B15	MCP_RGMII_VREF
RGMII_TXD0	F15	TP_ENET_TXD<0>
RGMII_TXD1	F17	TP_ENET_TXD<1>
RGMII_TXD2	J17	TP_ENET_TXD<2>
RGMII_TXD3	D15	TP_ENET_TXD<3>
RGMII_TXCLK	G14	TP_ENET_CLK125M_TXCLK
RGMII_TXCTL	C14	TP_ENET_TX_CTRL
RGMII_MDC	E15	TP_ENET_MDC
RGMII_MDIO	H18	ENET_MDIO
BUF_25MHZ	J14	TP_MCP_CLK25M_BUF0_R
RGMII_RESET*	G17	TP_ENET_RESET_L

=PP3V3_ENET_MCP_RMGT — R1810 49.9 1% 1/20W MF 201 — R1811 49.9 1% 1/20W MF 201

Internal MAC Disable:

Connect RGMII_RXD<0:3> together to 10K pull-down.
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
RGMII_COMP_VDD/_GND must remain connected as shown.
Connect RGMII_VREF to 10K pull-down.
Connect RGMII_MDIO to 10K pull-down.
All other pins can be left TP or NC.

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: MCP SATA, USB & Ethernet

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

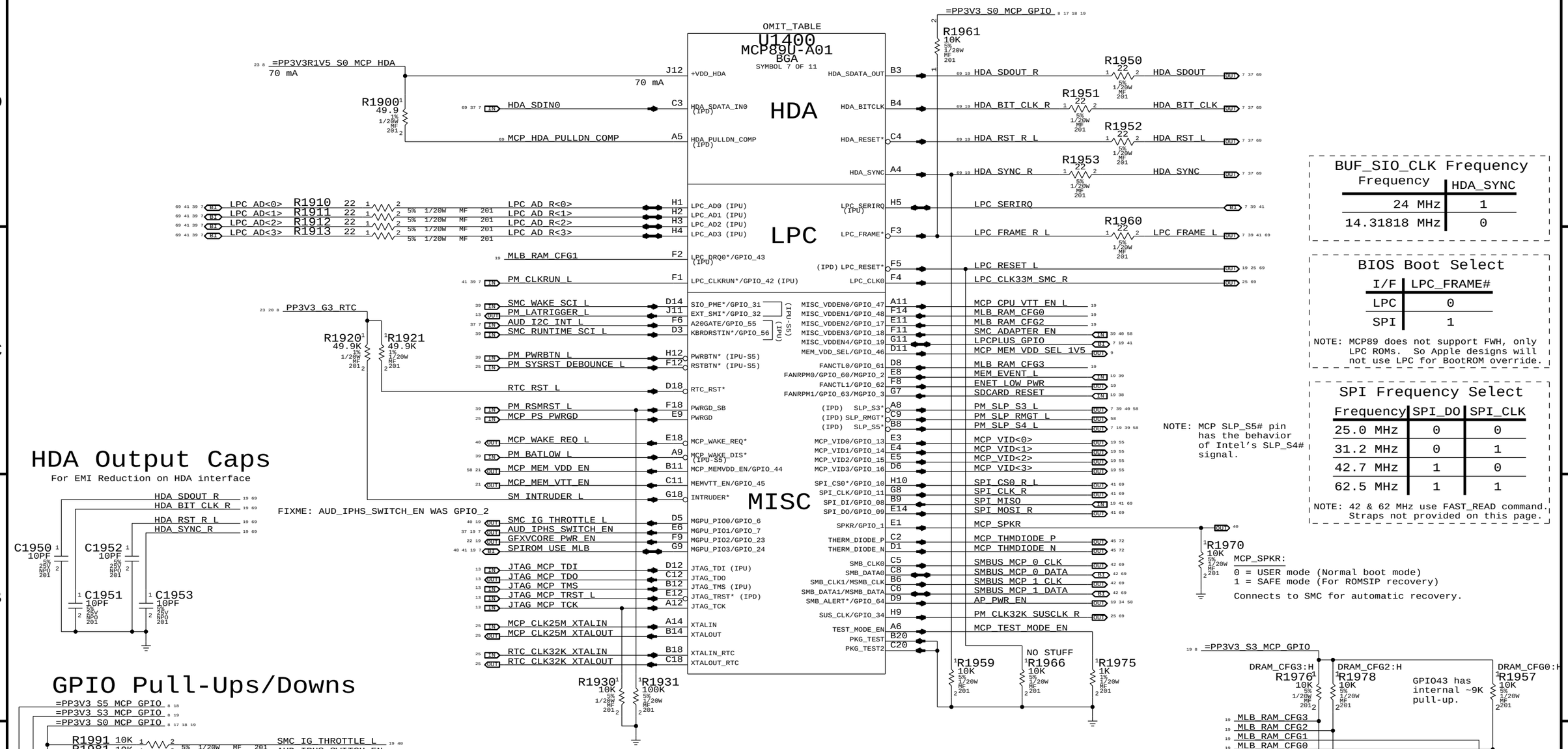
REVISION: 3.3.0

BRANCH

PAGE: 18 OF 110

SHEET: 18 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select

I/F	LPC_FRAME#
LPC	0
SPI	1

NOTE: MCP89 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command. Straps not provided on this page.

Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: MCP HDA, LPC & MISC

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

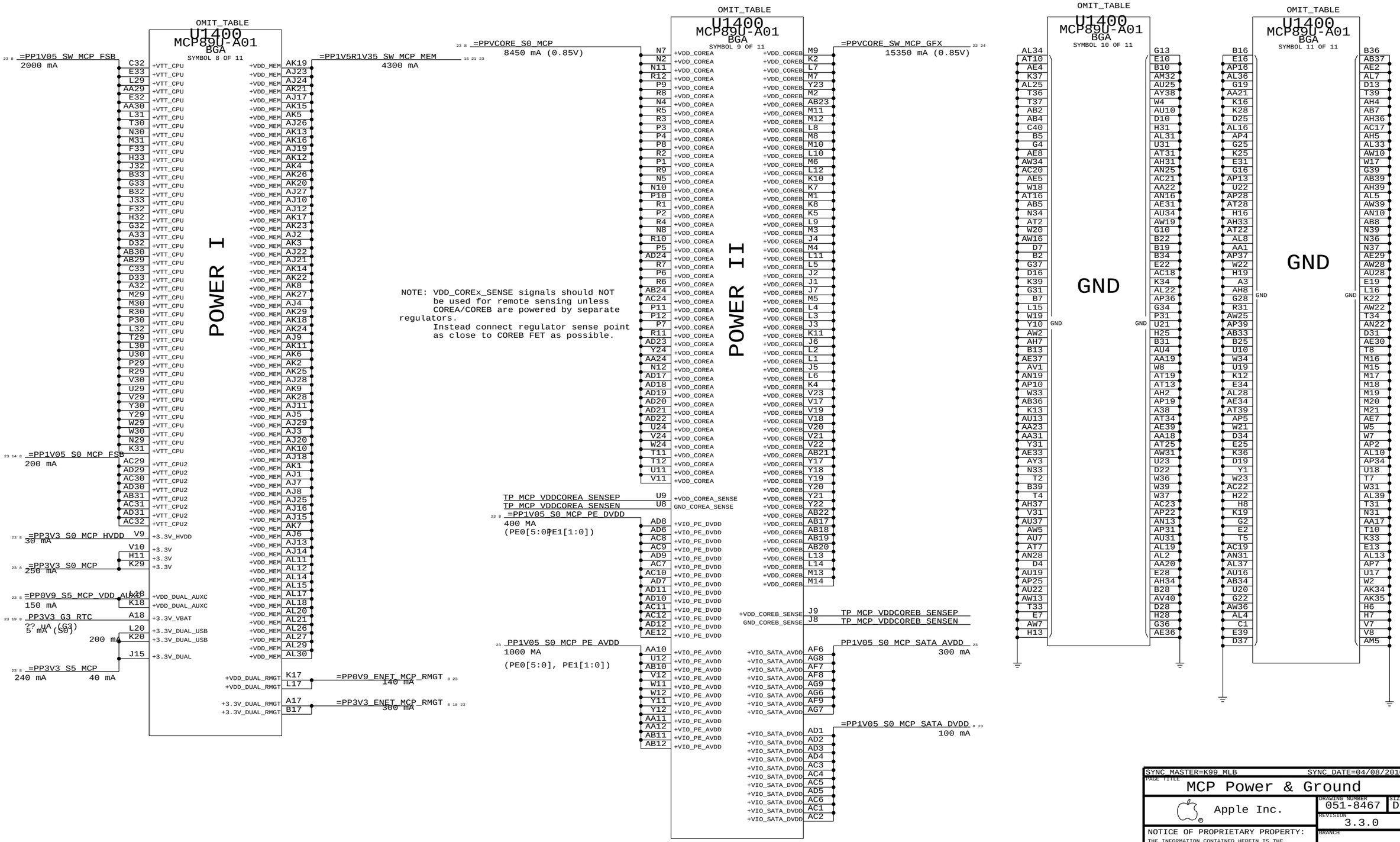
BRANCH

PAGE: 19 OF 110

SHEET: 19 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.



Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: MCP Power & Ground

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

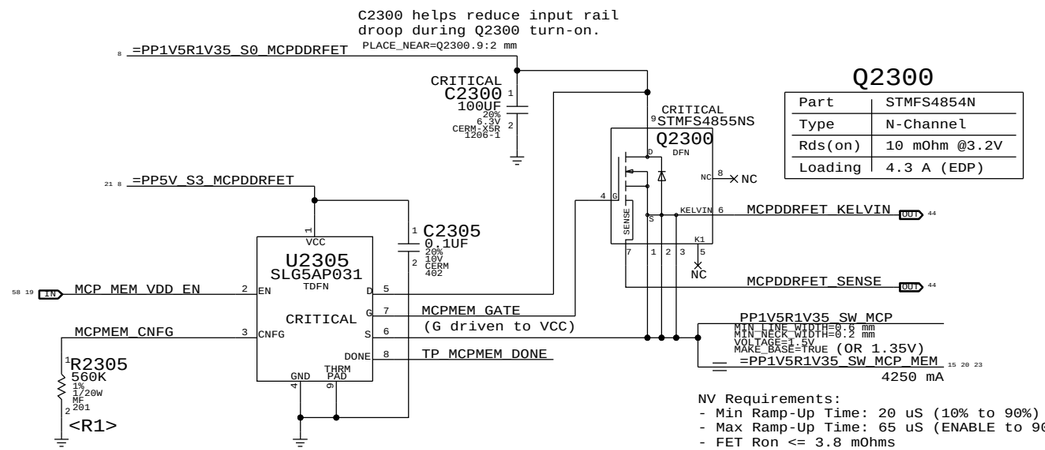
REVISION: 3.3.0

BRANCH

PAGE: 20 OF 110

SHEET: 20 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



Q2300

Part	STMFS4854N
Type	N-Channel
Rds(on)	10 mOhm @3.2V
Loading	4.3 A (EDP)

NV Requirements:
- Min Ramp-Up Time: 20 uS (10% to 90%)
- Max Ramp-Up Time: 65 uS (ENABLE to 90%)
- FET Ron <= 3.8 mOhms

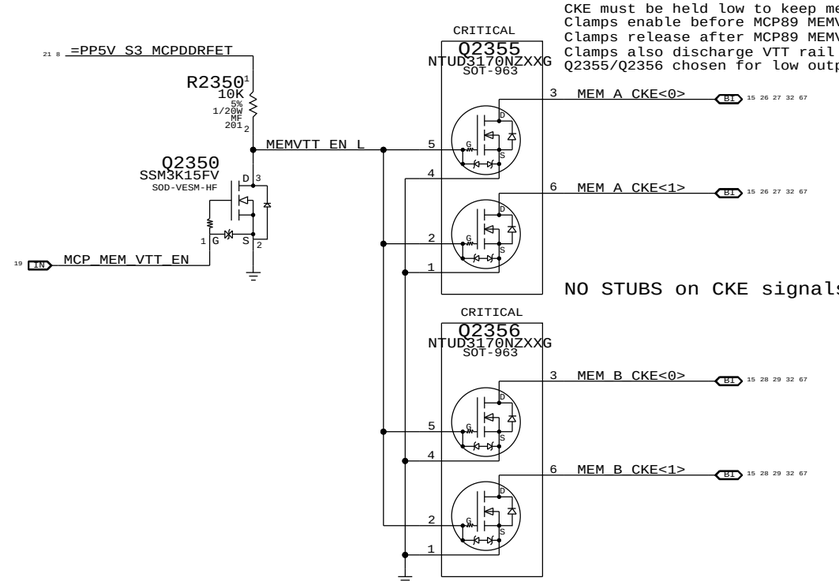
NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

Gated Rail Savings: 120mW

Approx. Ramp Time (EN to 1.35V, uS): 7.91 + 0.0678 * R1(Kohms)

DIMM CKE Clamps

CKE must be held low to keep memory in self-refresh.
Clamps enable before MCP89 MEMVDD rail switched off.
Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.
Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM.
Q2355/Q2356 chosen for low output capacitance.



NO STUBS on CKE signals!

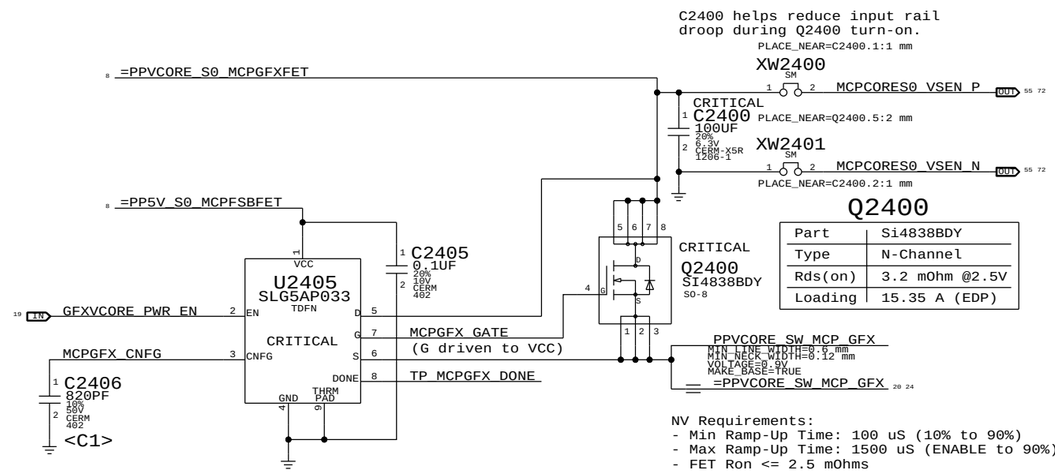
SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
MCP89 Memory Rail Gating

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 23 OF 110
SHEET 21 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



Q2400

Part	Si4838BDY
Type	N-Channel
Rds(on)	3.2 mOhm @2.5V
Loading	15.35 A (EDP)

Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

NV Requirements:
- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET Ron <= 2.5 mOhms

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

Gated Rail Savings: 860mW

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
MCP89 GFX Core Rail Gating

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

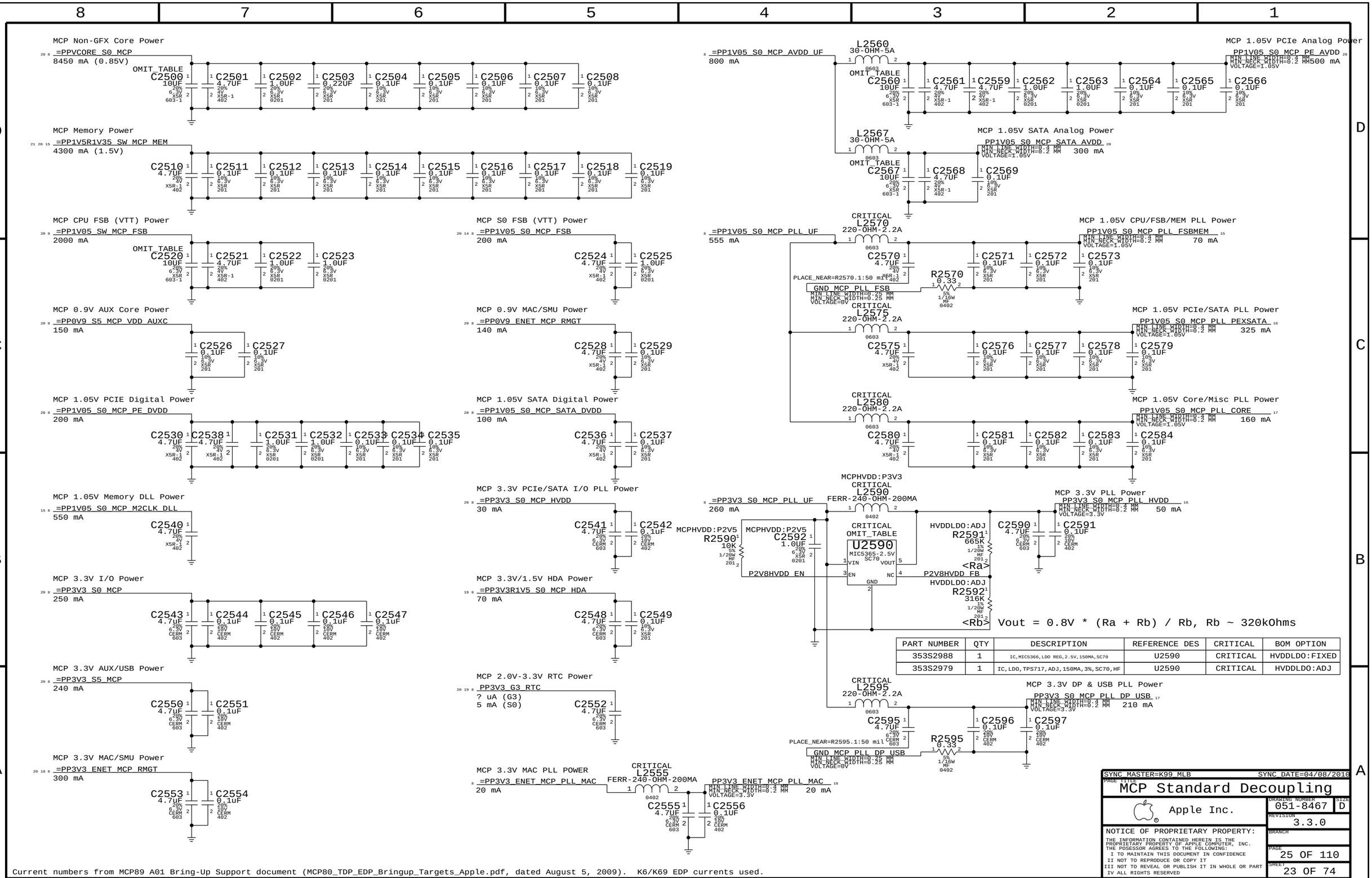
REVISION 3.3.0

BRANCH

PAGE 24 OF 110

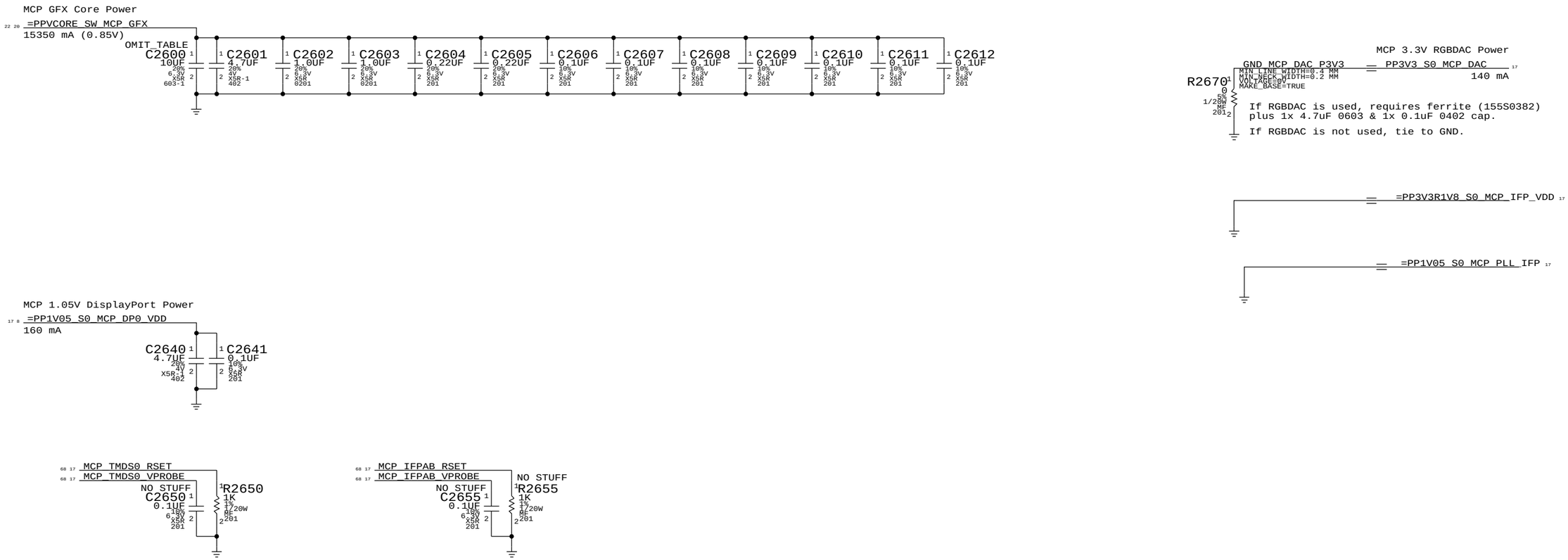
SHEET 22 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2988	1	IC,MIC5366,LDO REG,2.5V,150MA,SC70	U2590	CRITICAL	HVDDLDO:FIXED
353S2979	1	IC,LDO,TPS717,ADJ,150MA,3%,SC70,HF	U2590	CRITICAL	HVDDLDO:ADJ

Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.



Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

PAGE TITLE
MCP Graphics Support

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

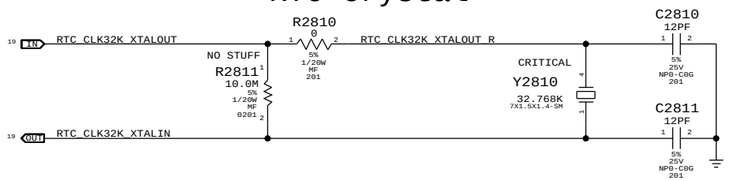
BRANCH

PAGE 26 OF 110

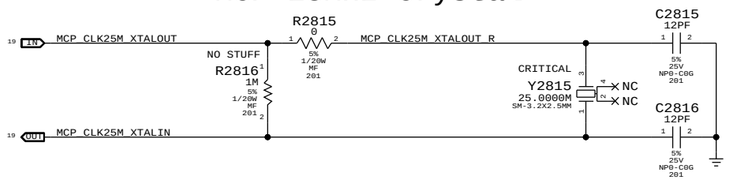
SHEET 24 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

RTC Crystal

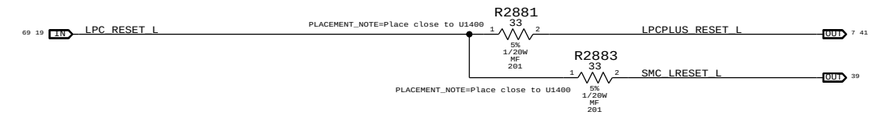


MCP 25MHz Crystal

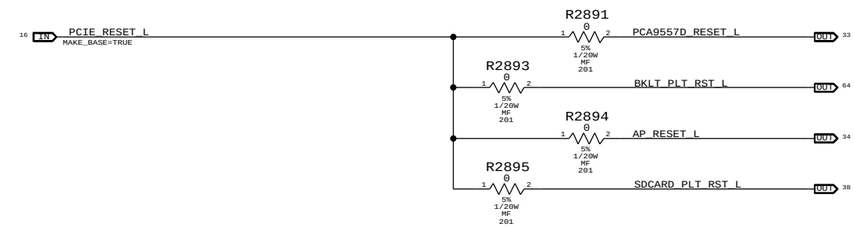


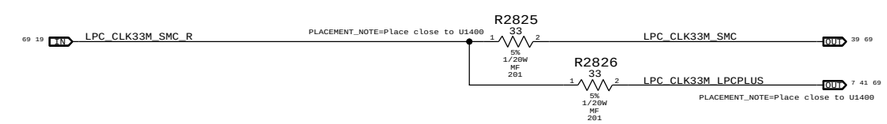
Platform Reset Connections

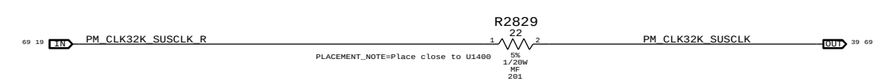
LPC Reset (Unbuffered)



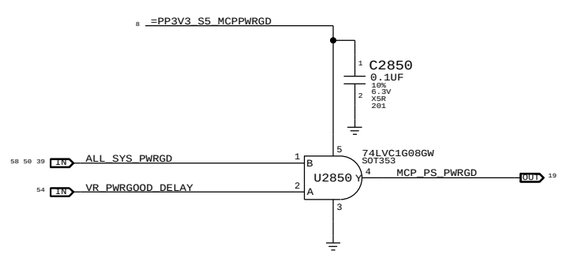
PCIE Reset (Unbuffered)



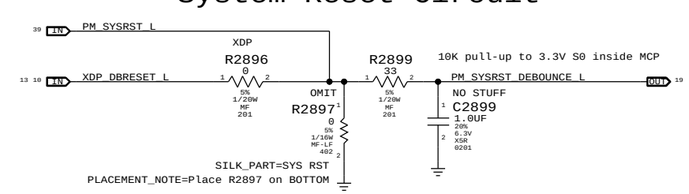




MCP S0 PWRGD & CPU_VLD



System Reset Circuit



SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/11/2010)

PAGE TITLE

SB Misc

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

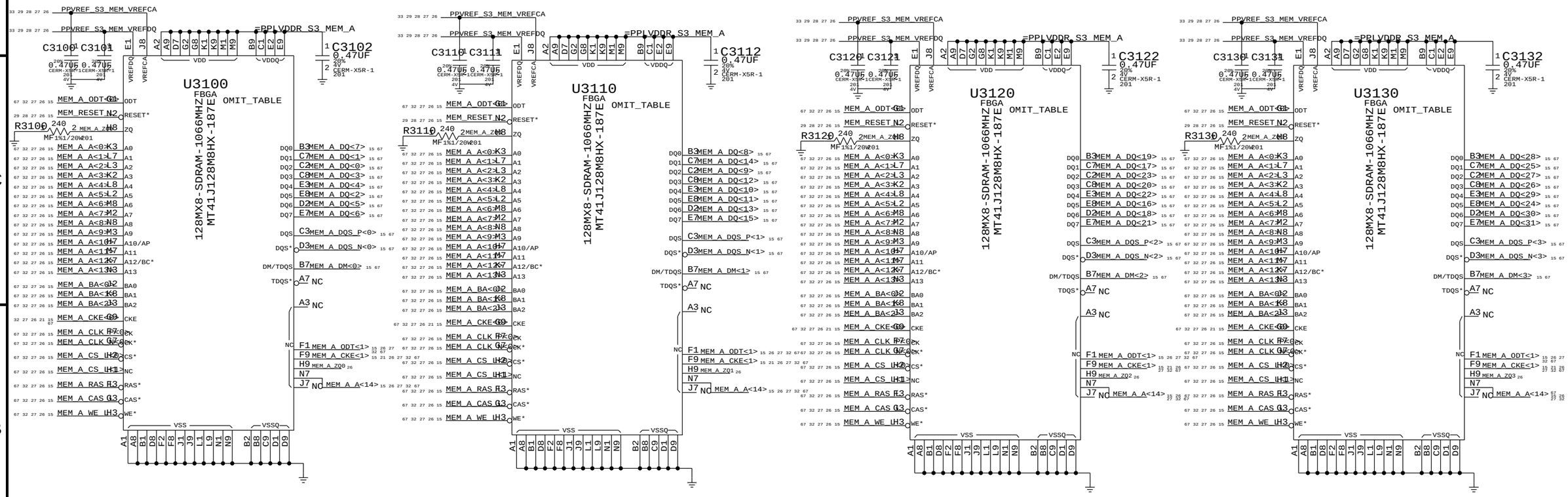
BRANCH

PAGE 28 OF 110

SHEET 25 OF 74

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
DDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

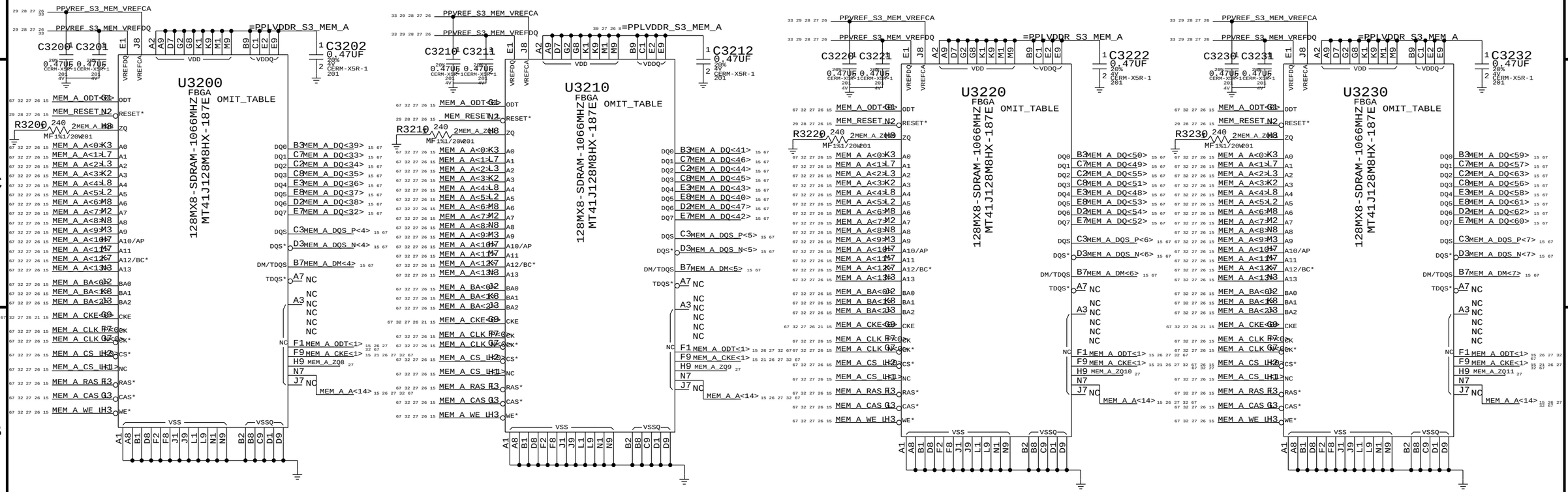
REVISION 3.3.0

BRANCH

PAGE 31 OF 110

SHEET 26 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

PAGE TITLE
DDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

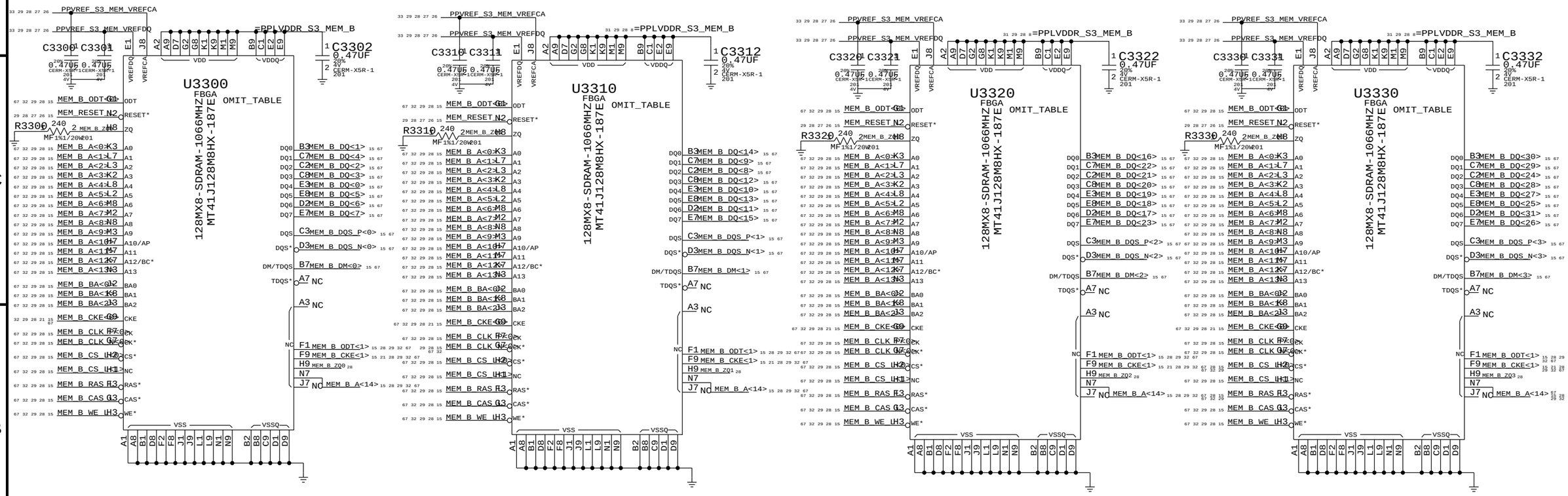
REVISION 3.3.0

BRANCH

PAGE 32 OF 110

SHEET 27 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
DDR3 DRAM Channel B (0-31)

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

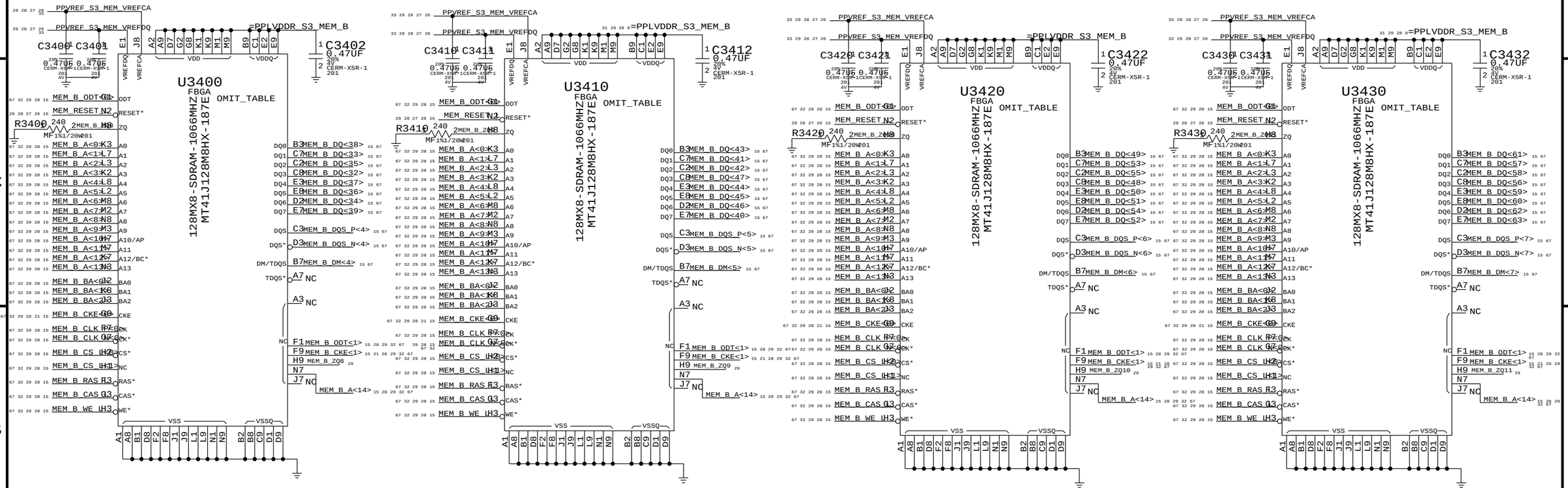
REVISION 3.3.0

BRANCH

PAGE 33 OF 110

SHEET 28 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
DDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

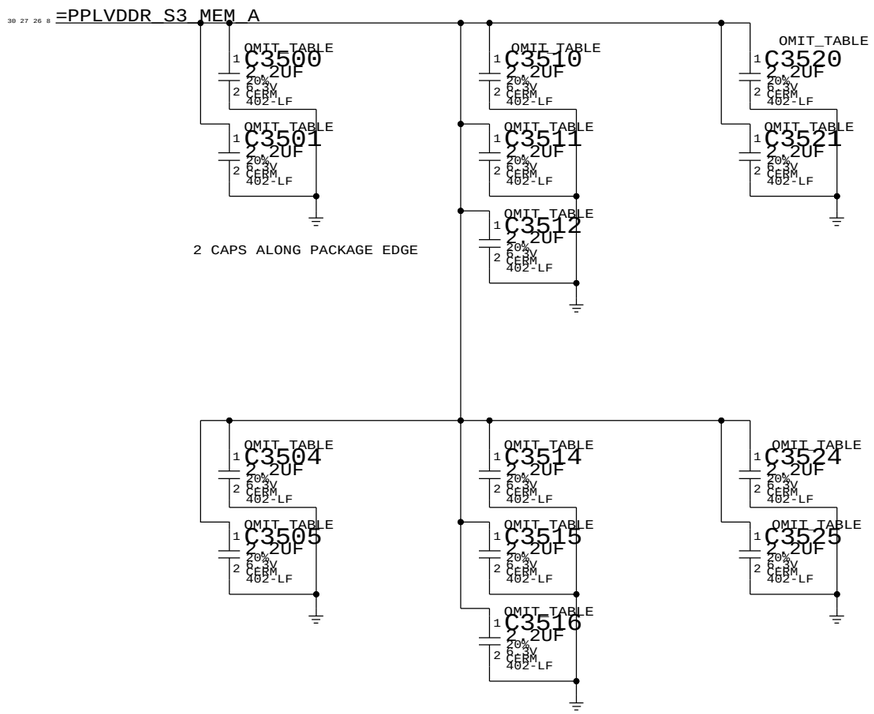
REVISION 3.3.0

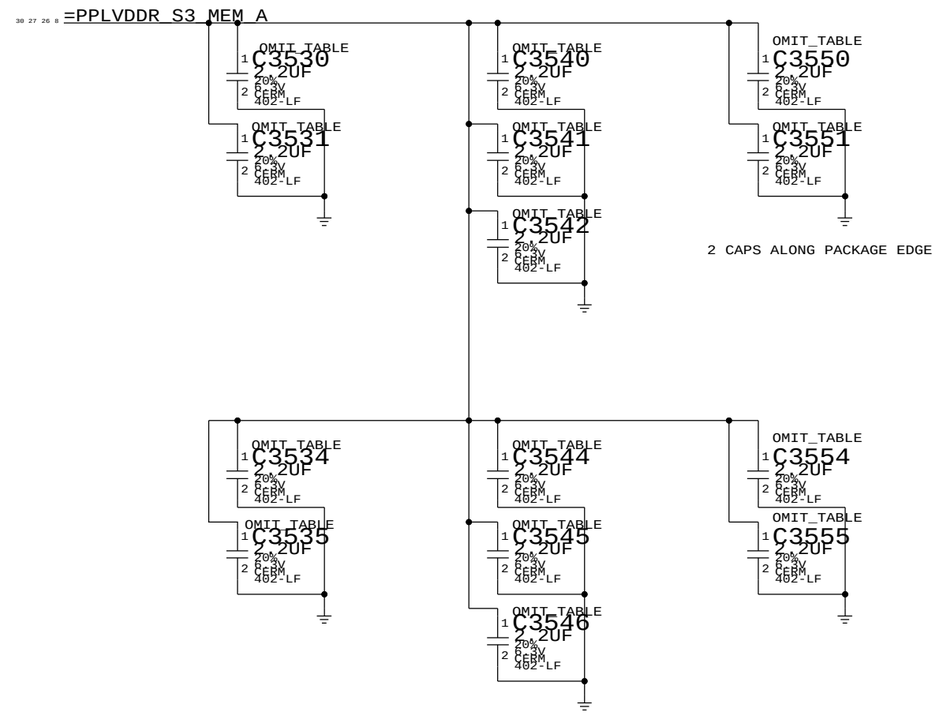
BRANCH

PAGE 34 OF 110

SHEET 29 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED





SYNC MASTER=K99_MLB SYNC DATE=04/08/2010

PAGE TITLE
DDR BYPASSING 1

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

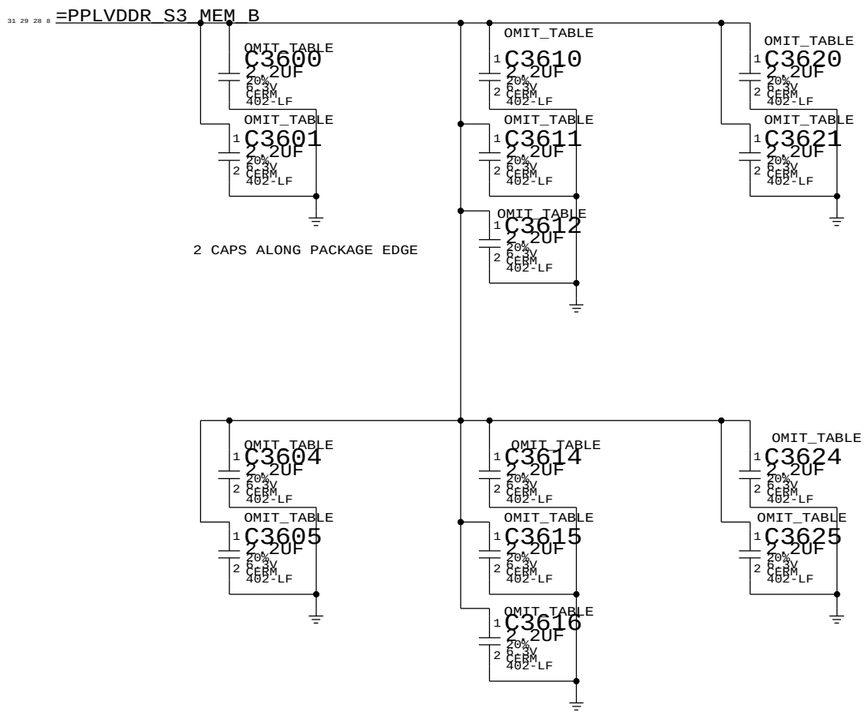
REVISION 3.3.0

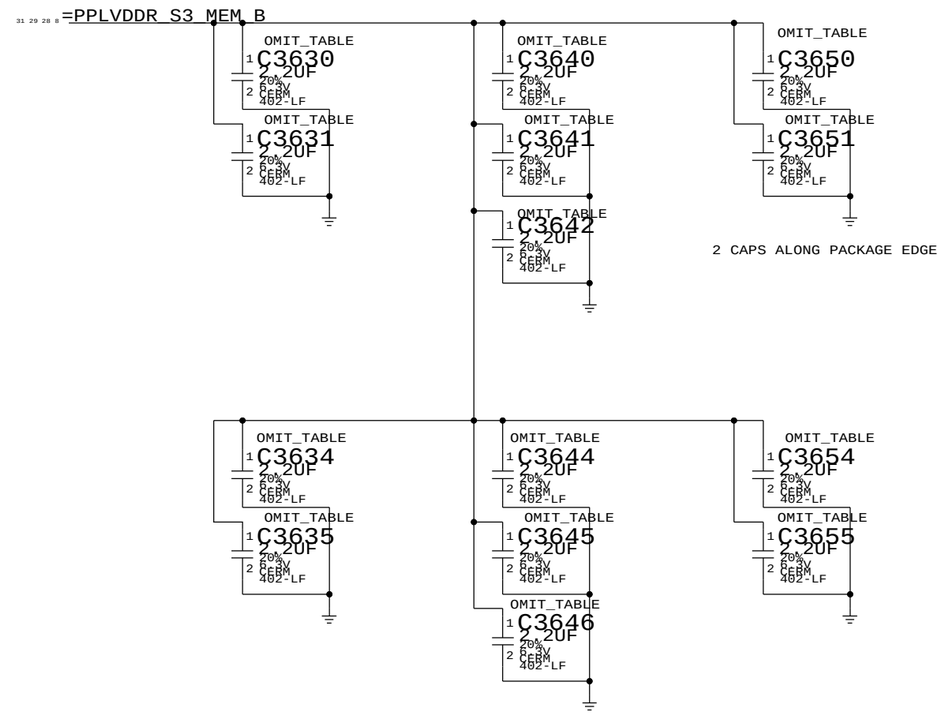
BRANCH

PAGE 35 OF 110

SHEET 30 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED





SYNC MASTER=K99_MLB SYNC DATE=04/08/2010

PAGE TITLE
DDR BYPASSING 2

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

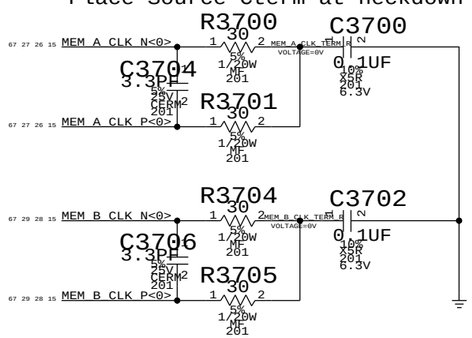
PAGE 36 OF 110

SHEET 31 OF 74

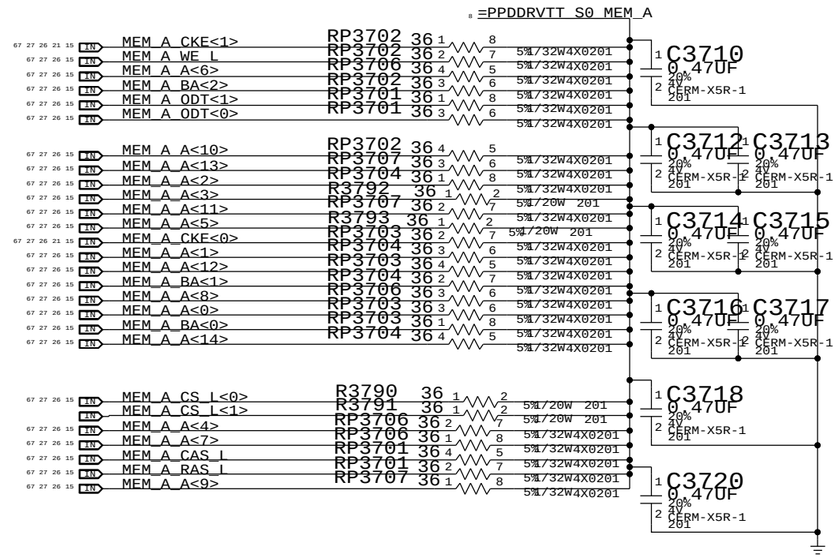
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

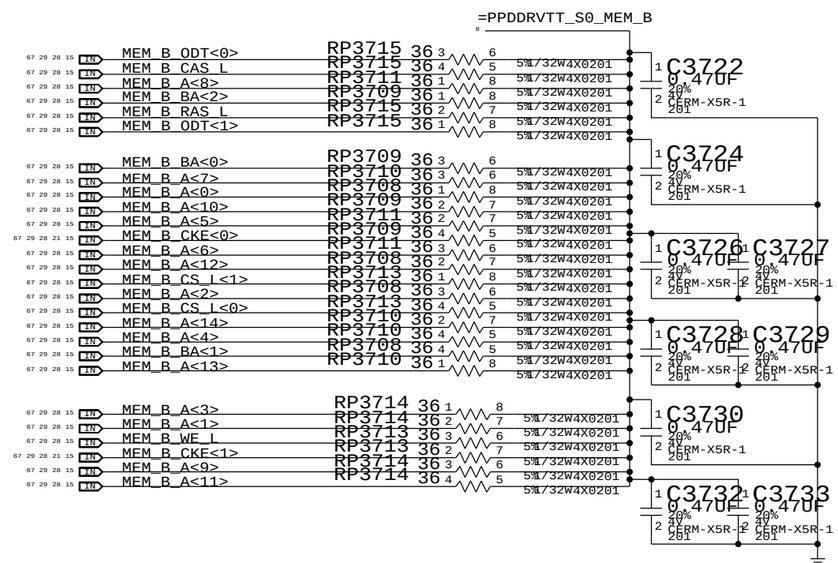
MEM CLOCK TERMINATION

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

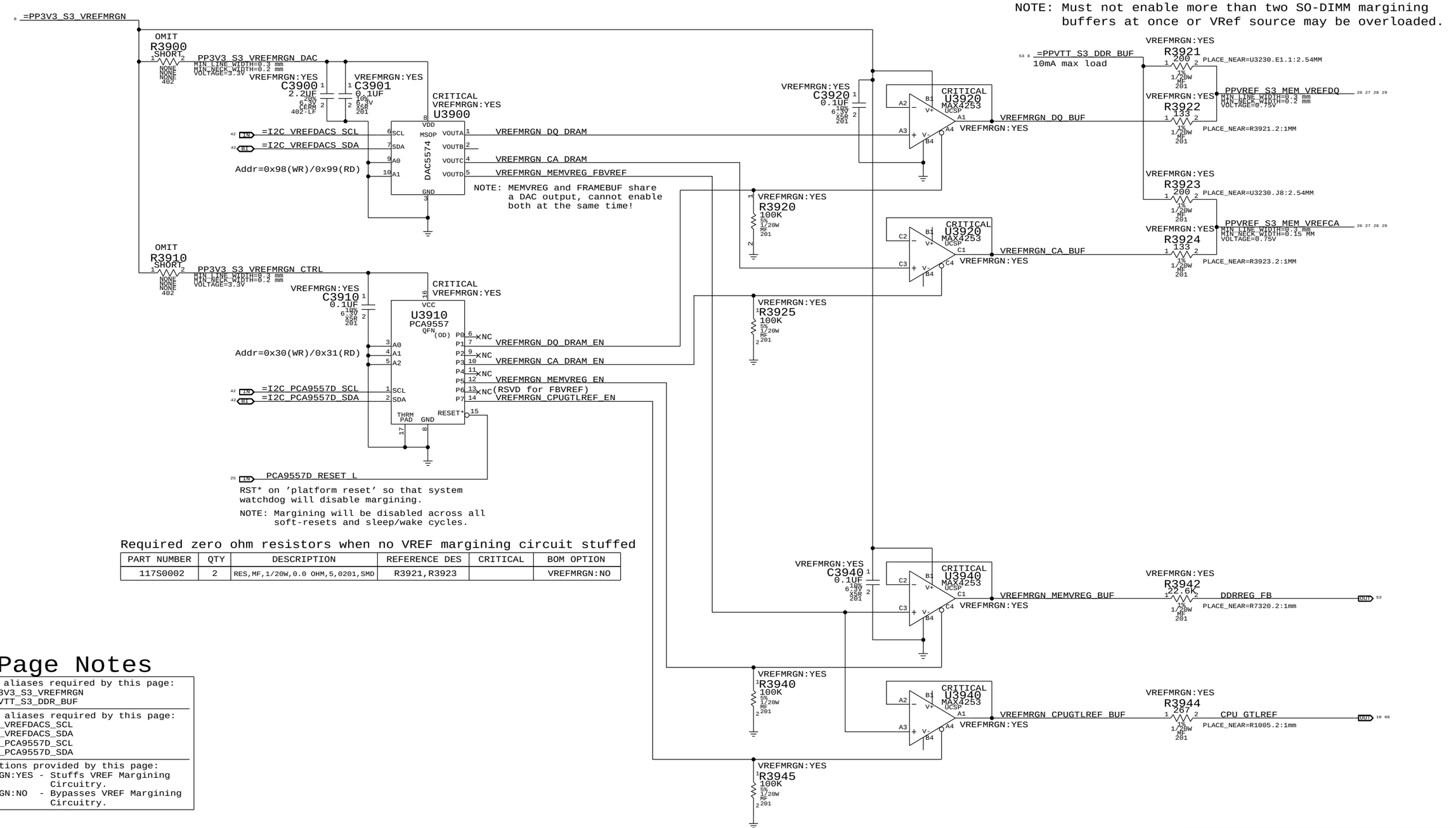
PAGE TITLE
Memory Active Termination

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 37 OF 110
SHEET 32 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3921,R3923		VREFMRGN:NO

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN:YES - Stuffs VREF Margining Circuitry.
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM VREF DQ	MEM VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	C	D	D
PCA9557D Pin:	1	3	5	7
Nominal value		0.75V (DAC: 0x3A)	1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)	1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
VRef current:		+3.4mA - -3.4mA (- = sourced)	+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output	8.59mV / step @ output	9.24mV / step @ output

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
FSB/DDR3 Vref Margining

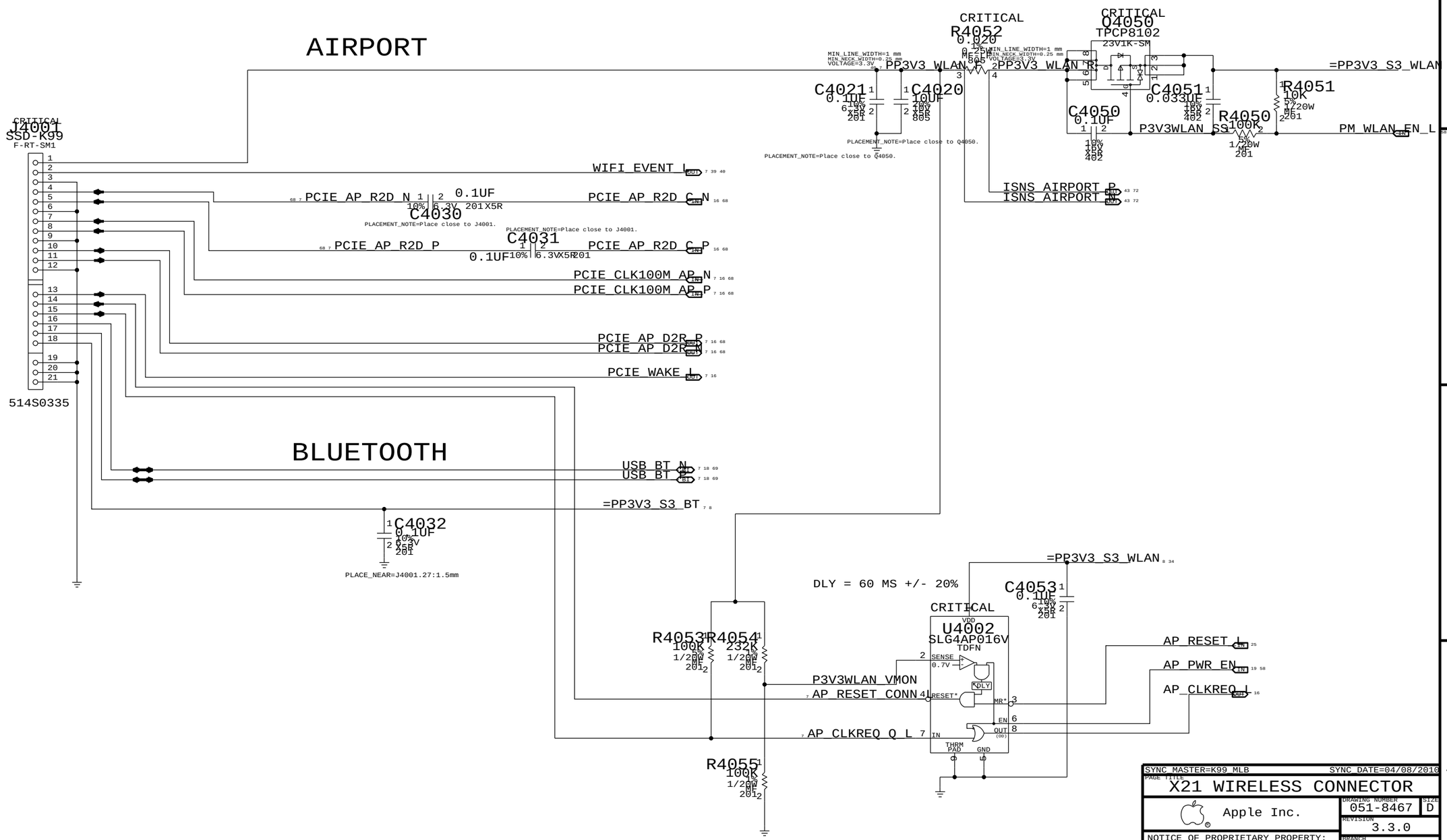
Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 39 OF 110
SHEET 33 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)



SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

PAGE TITLE
X21 WIRELESS CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

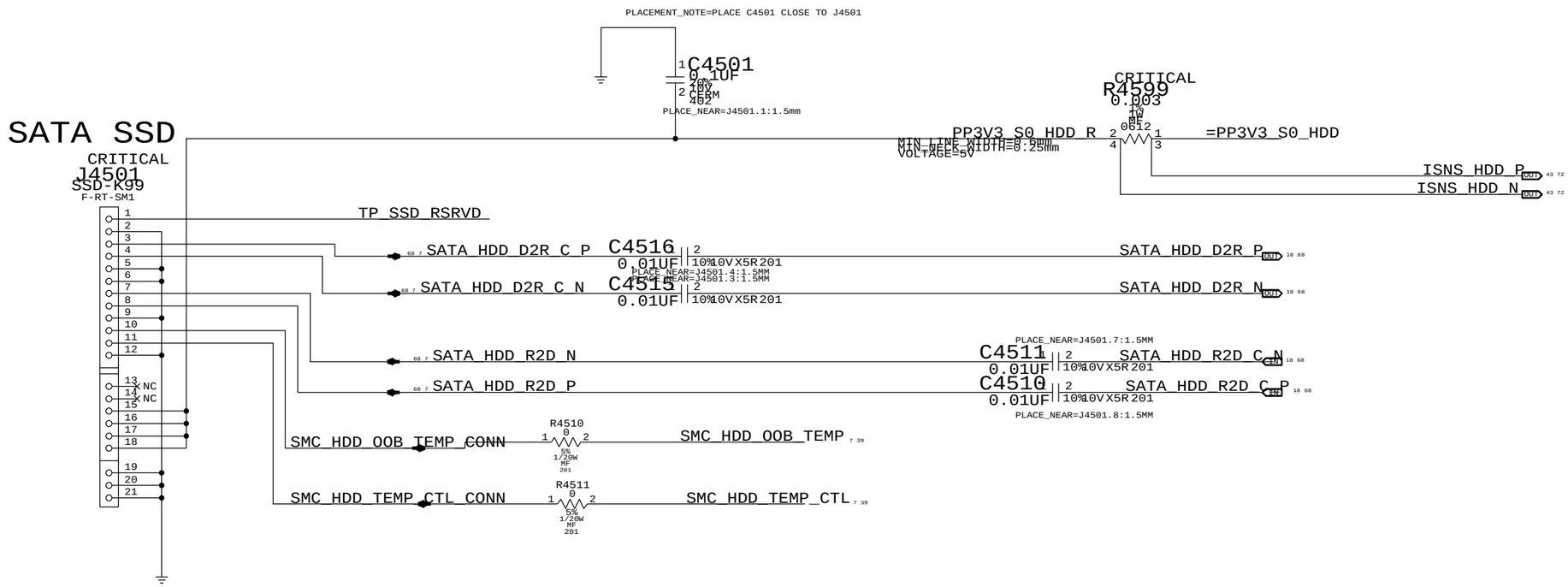
REVISION 3.3.0

BRANCH

PAGE 40 OF 110

SHEET 34 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE

SATA CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

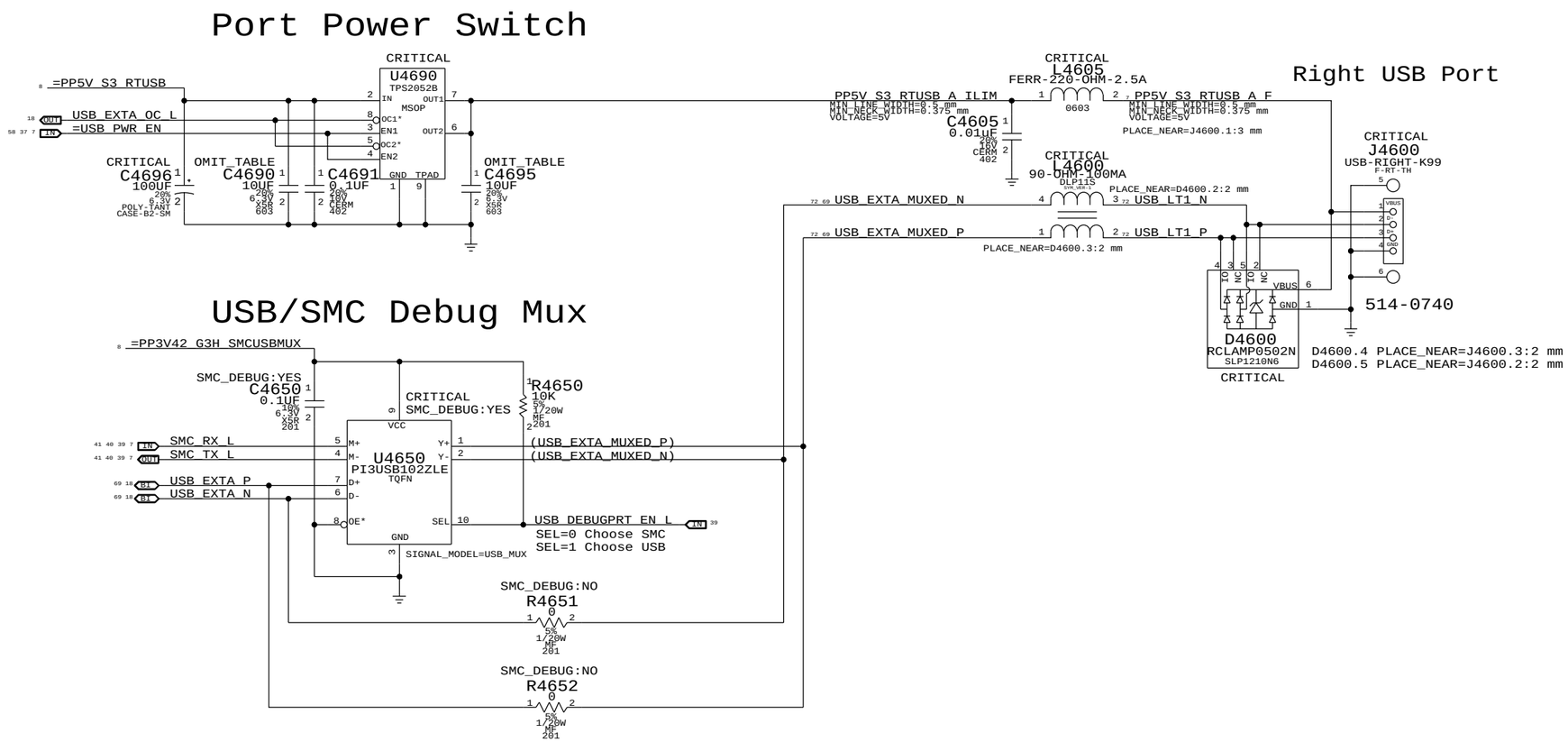
REVISION 3.3.0

BRANCH

PAGE 45 OF 110

SHEET 35 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=K99_MLB SYNC_DATE=03/01/2010

PAGE TITLE
External USB Connectors

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

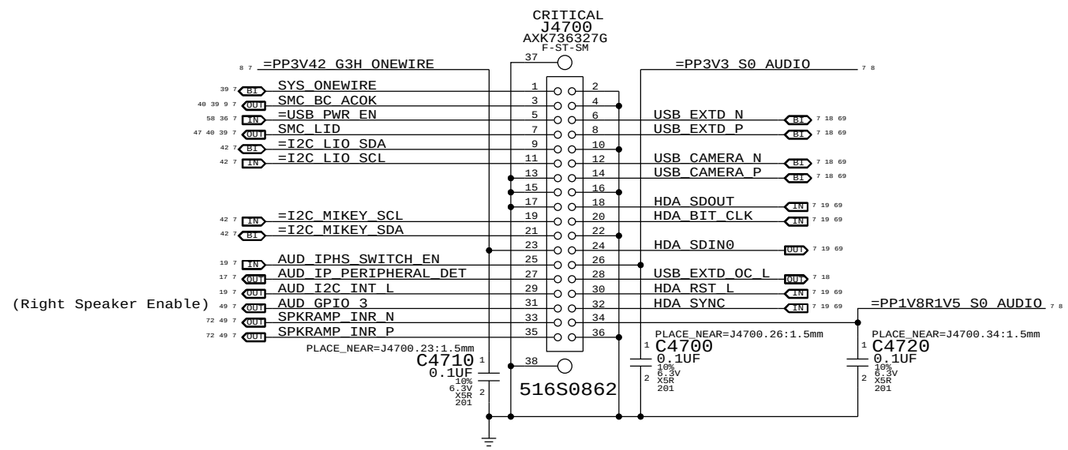
REVISION 3.3.0

BRANCH

PAGE 46 OF 110

SHEET 36 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE
Left I/O (LIO) Connector

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

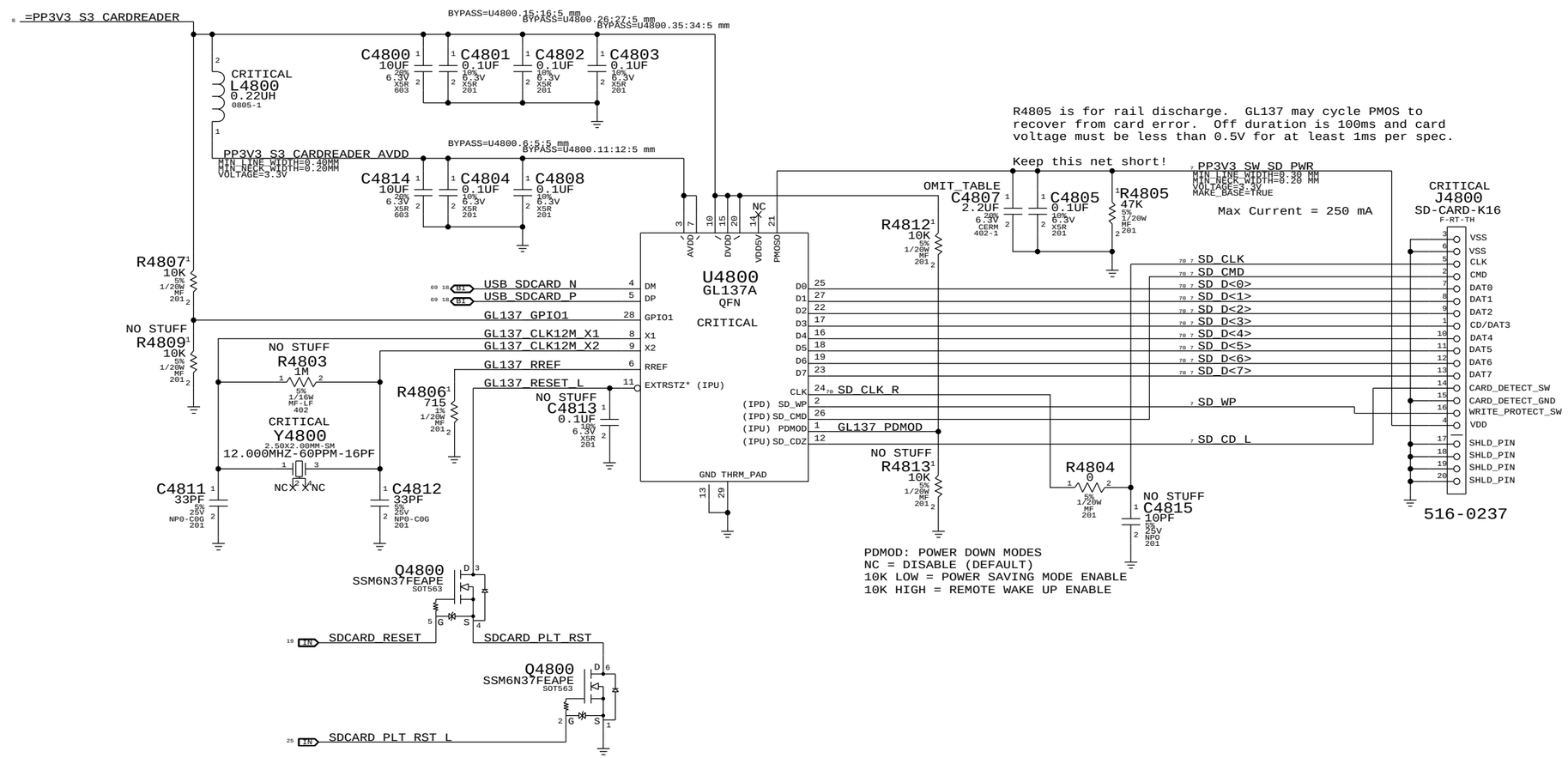
REVISION 3.3.0

BRANCH

PAGE 47 OF 110

SHEET 37 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

PAGE TITLE
SecureDigital Card Reader

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

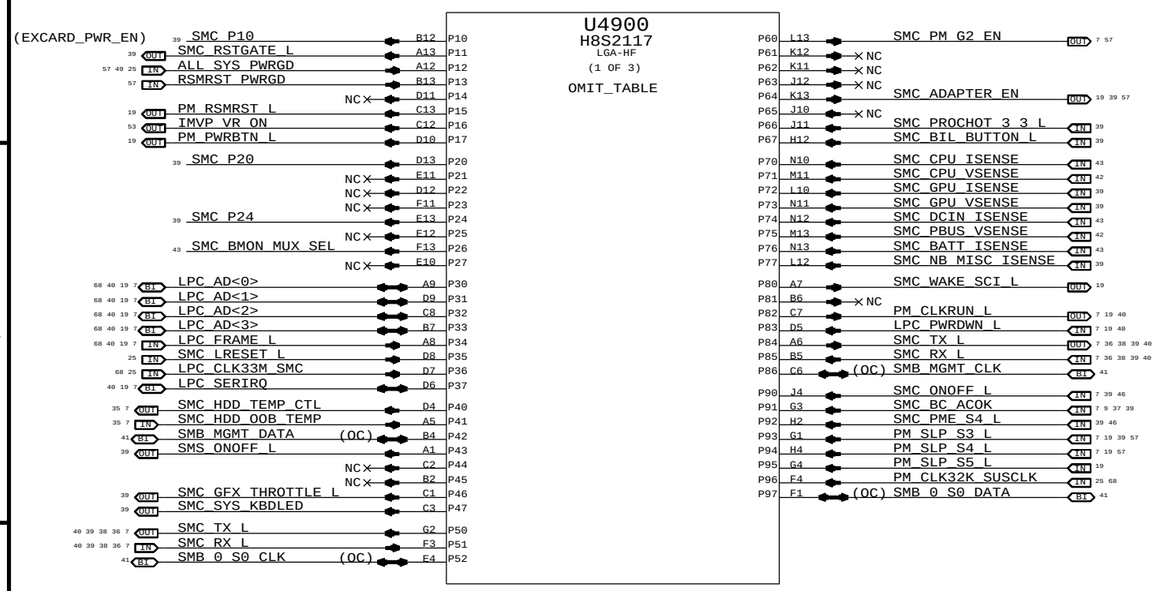
BRANCH

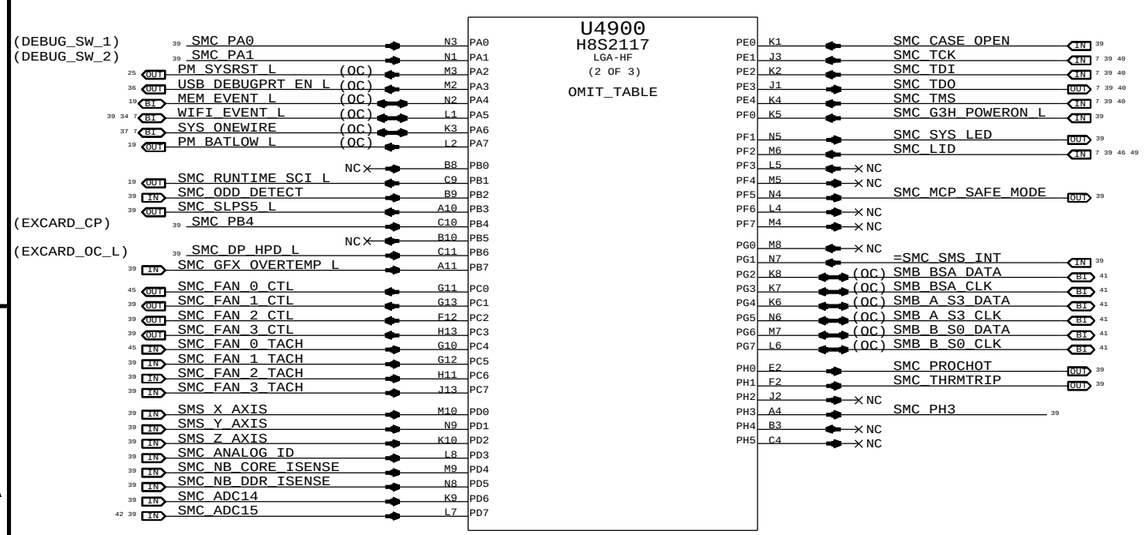
PAGE 48 OF 110

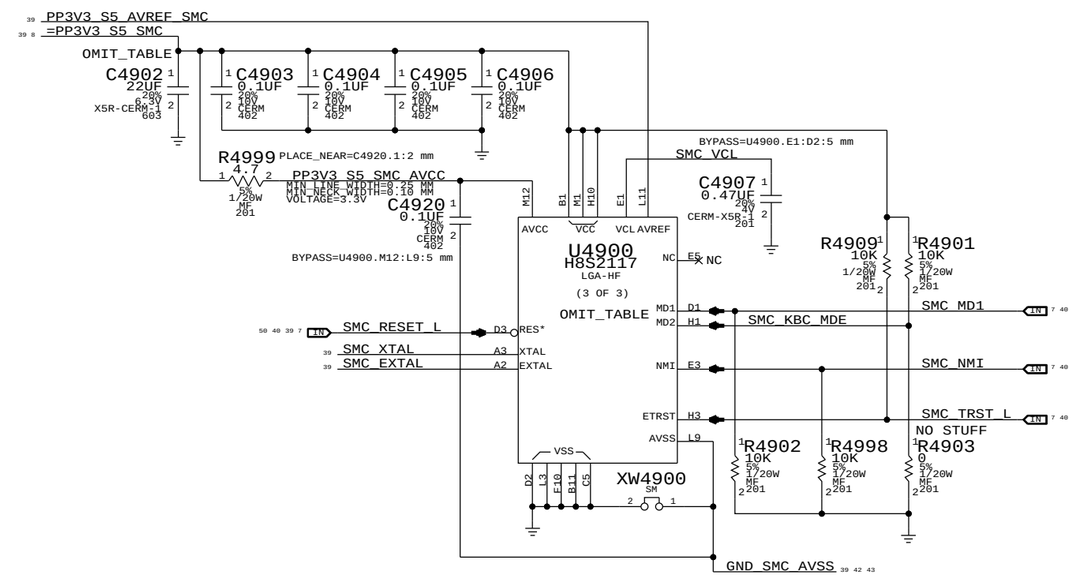
SHEET 38 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designed as inputs require pull-ups.







NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

H8S2117-R:
(SMC_PECI)
(SMC_PECI_VREF)
(SMC_PECI_VSTP)

SYNC_MASTER=K16_MLB SYNC_DATE=06/01/2010

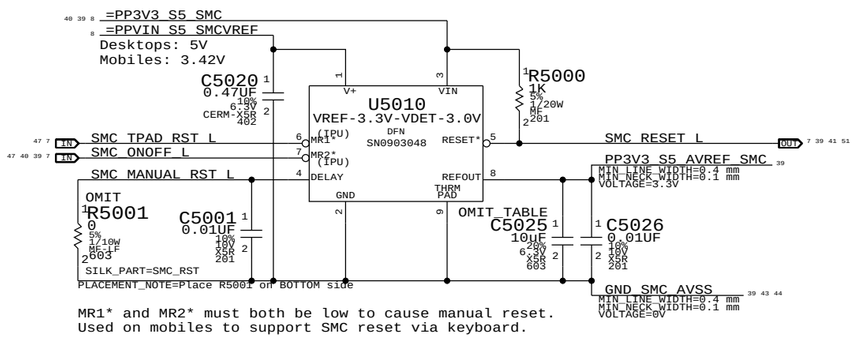
PAGE TITLE
SMC

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 49 OF 110
SHEET 39 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

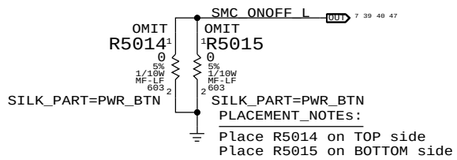
SMC Reset "Button", Supervisor & AVREF Supply



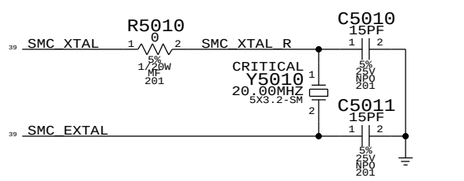
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

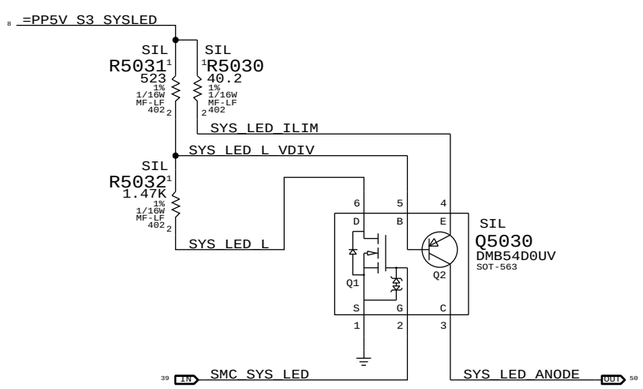
Debug Power "Buttons"



SMC Crystal Circuit



System (Sleep) LED Circuit



SMC Aliases

SMC_LCDBKLT_ISENSE (MAKE_BASE=TRUE)	—	SMS_X_AXIS	OUT
SMC_WLAN_ISENSE (MAKE_BASE=TRUE)	—	SMS_Y_AXIS	OUT
SMC_HDD_ISENSE (MAKE_BASE=TRUE)	—	SMS_Z_AXIS	OUT
SMC_CSREG_ISENSE (MAKE_BASE=TRUE)	—	SMC_ADC14	OUT
SMC_LCDBKLT_VSENSE	—	SMC_ADC15	OUT
SMC_MCP_CORE_ISENSE (MAKE_BASE=TRUE)	—	SMC_NB_CORE_ISENSE	OUT
SMC_MCP_DDR_ISENSE (MAKE_BASE=TRUE)	—	SMC_NB_DDR_ISENSE	OUT
SMC_1V5S3_ISENSE (MAKE_BASE=TRUE)	—	SMC_NB_MISC_ISENSE	OUT
TP_SMC_ANALOG_ID (MAKE_BASE=TRUE)	—	SMC_ANALOG_ID	OUT
TP_SMC_GPU_ISENSE (MAKE_BASE=TRUE)	—	SMC_GPU_ISENSE	OUT
SMC_MCP_VSENSE (MAKE_BASE=TRUE)	—	SMC_GPU_VSENSE	OUT
SMC_GFX_THROTTLE_L	—	SMC_IG_THROTTLE_L (MAKE_BASE=TRUE)	OUT
SMS_INT_L (MAKE_BASE=TRUE)	—	=SMC_SMS_INT	IN
MCP_WAKE_REQ_L	—	SMC_G3H_POWERON_L (MAKE_BASE=TRUE)	OUT

R5096 0: SMC_MCP_SAFE_MODE — MCP_SPKR

DP_PWR:S0 R5020 0: PM_SLP_S3_L — DP_PWR_EN (MAKE_BASE=TRUE) — =DP_PWR_EN

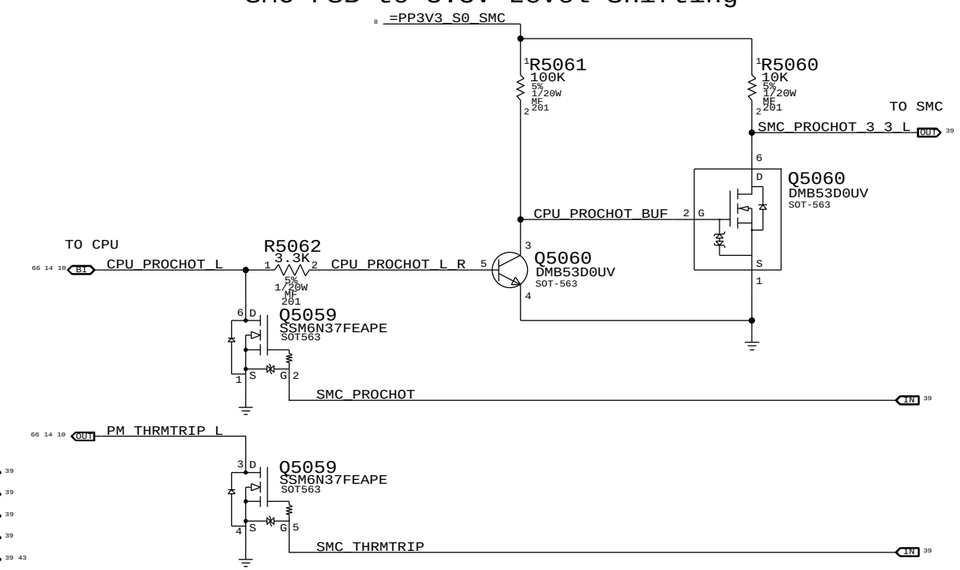
DP_PWR:SMC R5021 0: SMC_SLPS5_L

DP_PWR:SMC R5022 0: SMC_DP_HPD_L — DP_EXT_HPD_L (PLACE_NEAR=Q9441.2:5 mm)

Unused Pins

SMS_ONOFF_L	—	TP_SMS_ONOFF_L (MAKE_BASE=TRUE)	
SMC_SYS_KBDLED	—	TP_SMC_SYS_KBDLED (MAKE_BASE=TRUE)	
SMC_FAN_1_CTL	—	TP_SMC_FAN_1_CTL (MAKE_BASE=TRUE)	
TP_SMC_FAN_1_TACH (MAKE_BASE=TRUE)	—	SMC_FAN_1_TACH	OUT
SMC_FAN_2_CTL	—	NC_SMC_FAN_2_CTL (MAKE_BASE=TRUE NO_TEST=TRUE)	
NC_SMC_FAN_2_TACH (MAKE_BASE=TRUE NO_TEST=TRUE)	—	SMC_FAN_2_TACH	OUT
SMC_FAN_3_CTL	—	NC_SMC_FAN_3_CTL (MAKE_BASE=TRUE NO_TEST=TRUE)	
NC_SMC_FAN_3_TACH (MAKE_BASE=TRUE NO_TEST=TRUE)	—	SMC_FAN_3_TACH	OUT
SMC_RSTGATE_L	—	TP_SMC_RSTGATE_L (MAKE_BASE=TRUE)	
SMC_P10	—	TP_SMC_P10 (MAKE_BASE=TRUE)	
SMC_P20	—	TP_SMC_P20 (MAKE_BASE=TRUE)	
SMC_P24	—	TP_SMC_P24 (MAKE_BASE=TRUE)	
SMC_PH3	—	TP_SMC_PH3 (MAKE_BASE=TRUE)	

SMC FSB to 3.3V Level Shifting



SMC Pull-ups

=PP3V3_S5_SMC

SMC_PA0	R5091	100K	5% 1/20W MF 201
SMC_PA1	R5092	100K	5% 1/20W MF 201
SMC_PB4	R5088	10K	5% 1/20W MF 201
SMC_ONOFF_L	R5070	10K	5% 1/20W MF 201
SMC_LID	R5071	100K	5% 1/20W MF 201
SMC_TX_L	R5073	10K	5% 1/20W MF 201
SMC_RX_L	R5074	100K	5% 1/20W MF 201
SMC_TMS	R5077	10K	5% 1/20W MF 201
SMC_TDO	R5078	10K	5% 1/20W MF 201
SMC_TDI	R5079	10K	5% 1/20W MF 201
SMC_TCK	R5080	10K	5% 1/20W MF 201
SMC_ODD_DETECT	R5040	10K	5% 1/20W MF 201
SMC_BIL_BUTTON_L	R5081	10K	5% 1/20W MF 201
SMC_BC_ACOK	R5087	470K	5% 1/20W MF 201
SMC_GFX_OVERTEMP_L	R5094	10K	5% 1/20W MF 201
SMC_G3H_POWERON_L	R5098	100K	5% 1/20W MF 201
SMS_INT_L	R5093	10K	5% 1/20W MF 201
WIFI_EVENT_L (PP3V3_WLAN_F, NO STUFF)	R5089	10K	5% 1/20W MF 201
SMC_PME_S4_L (=PP3V3_SMC_PME)	R5076	100K	5% 1/20W MF 201

SMC Pull-downs

SMC_ADAPTER_EN	R5085	10K	5% 1/20W MF 201
SMC_CASE_OPEN	R5086	10K	5% 1/20W MF 201
SMC_DP_HPD_L (DP_PWR:S0)	R5090	100K	5% 1/20W MF 201

SYNC_MASTER=(K99_MLB) SYNC_DATE=(03/01/2010)

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

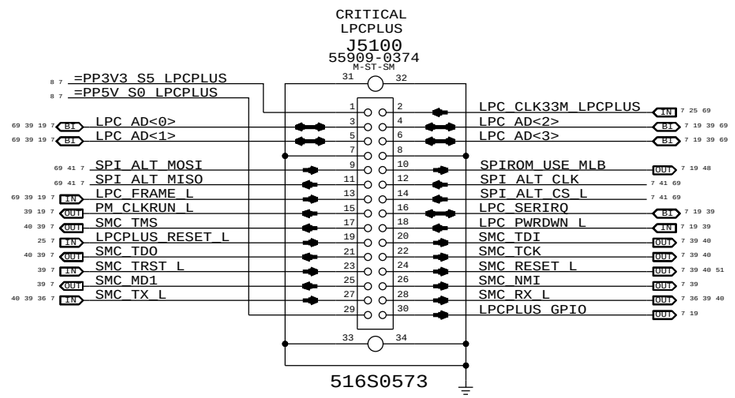
BRANCH

PAGE: 50 OF 110

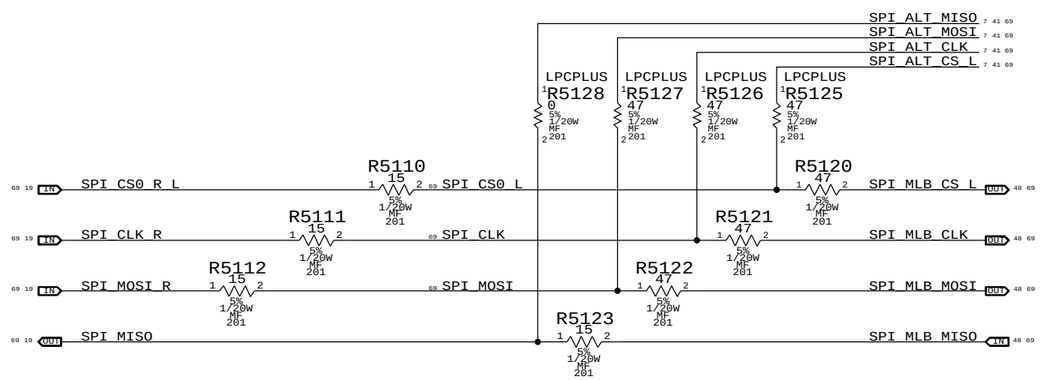
SHEET: 40 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

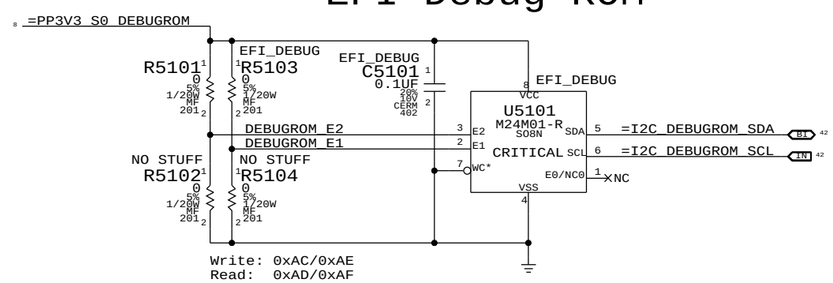
LPC+SPI Connector



SPI Bus Series Termination



EFI Debug ROM



EFI_DEBUG

SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

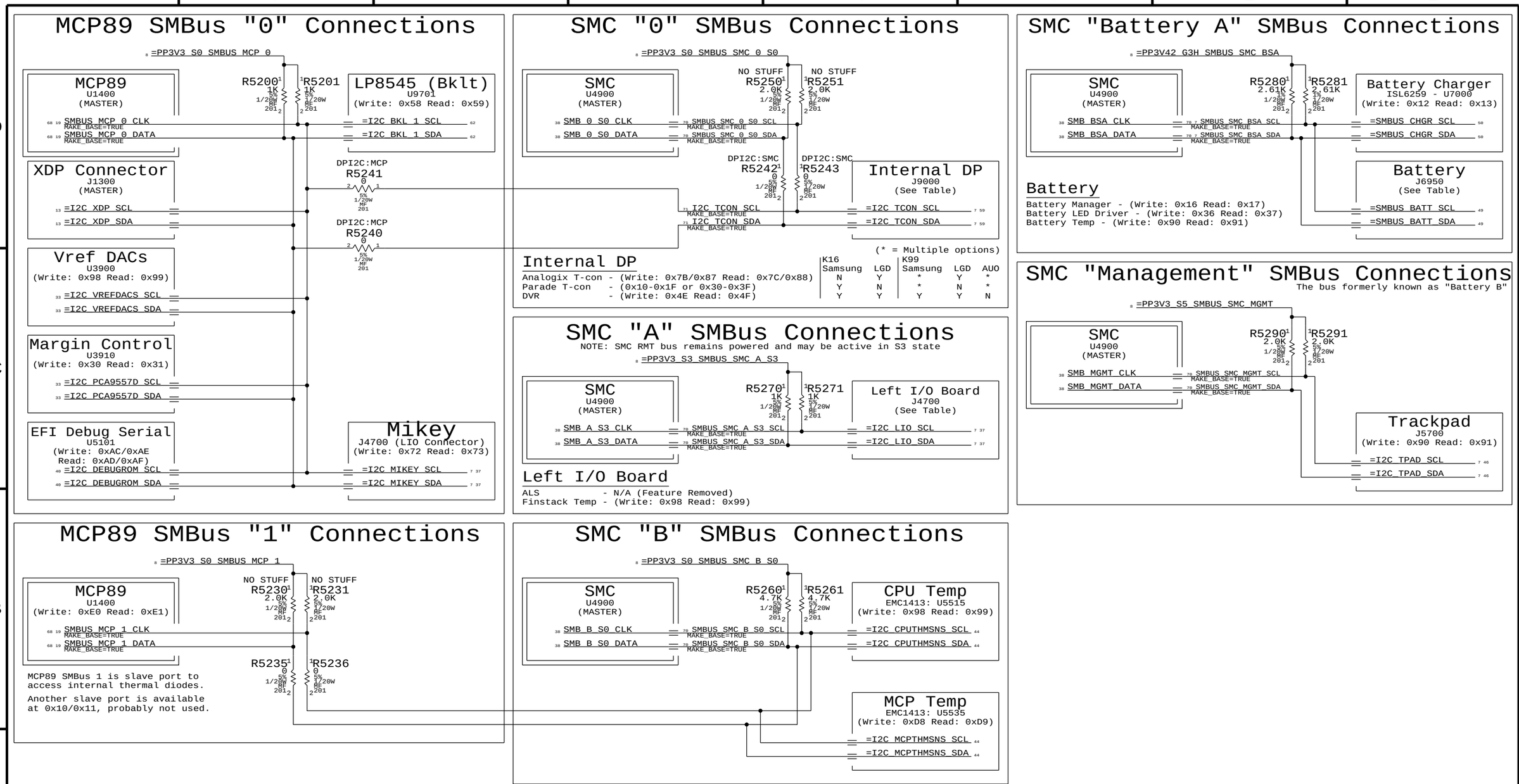
REVISION 3.3.0

BRANCH

PAGE 51 OF 110

SHEET 41 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=K99_MLB SYNC_DATE=07/23/2010

PAGE TITLE
K16/K99 SMus Connections

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

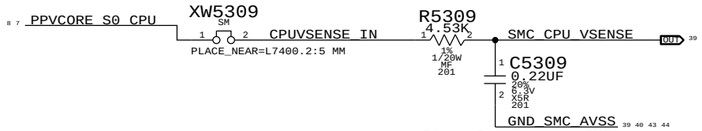
BRANCH

PAGE 52 OF 110

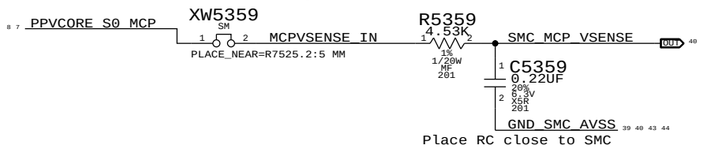
SHEET 42 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

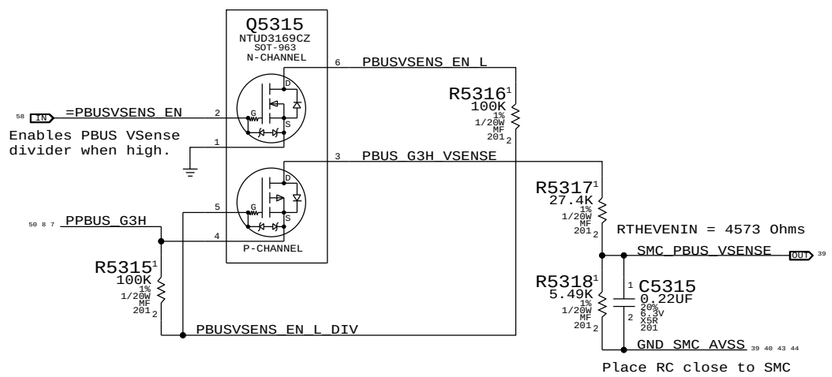
CPU Voltage Sense / Filter



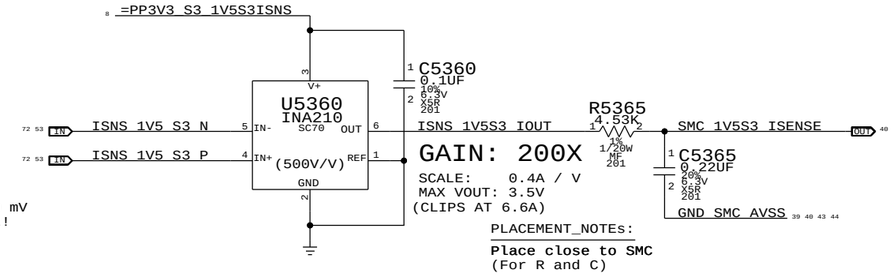
MCP Voltage Sense / Filter



PBUS Voltage Sense Enable & Filter

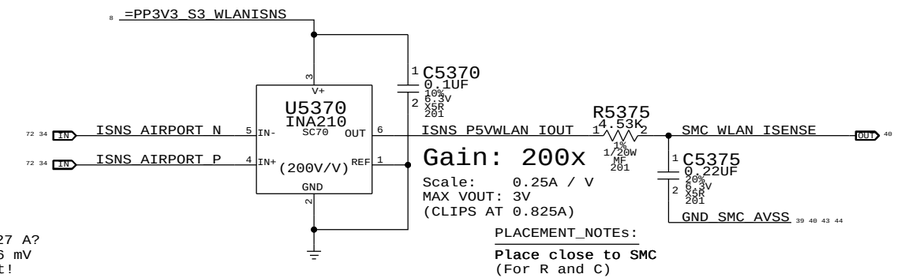


DDR3 1V5R1V35 Current Sense / Filter



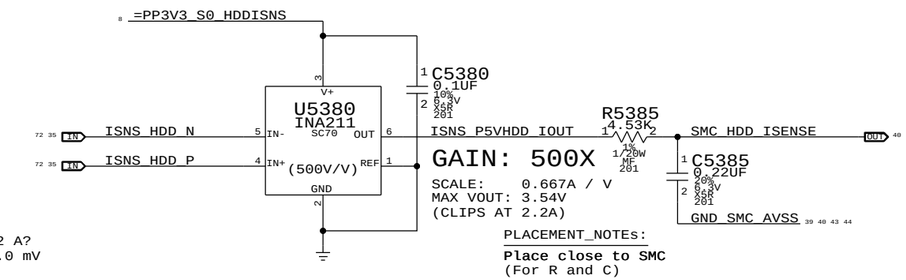
EDP Current: 7 A
Max Vdiff: 13.0 mV
WF: Verify SO-DIMM current!

AirPort Current Sense / Filter



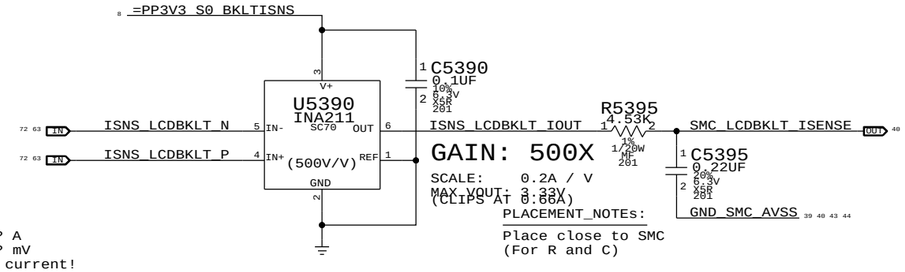
EDP Current: 0.727 A?
Max Vdiff: 14.6 mV
WF: Verify Airport current!

HDD Current Sense / Filter

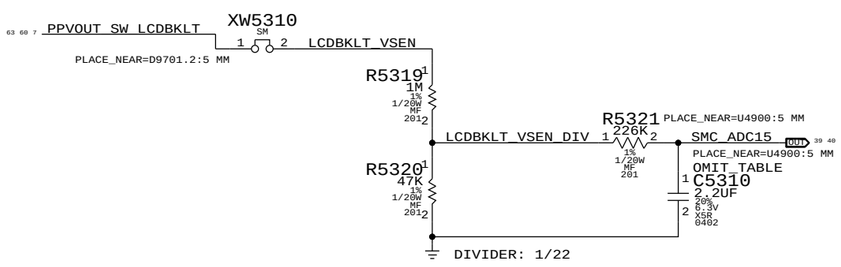


EDP Current: 1.2 A?
Max Vdiff: 24.0 mV
WF: Verify SSD current!

LCD Backlight Driver Input Current Sense / Filter



EDP Current: ??? A
Max Vdiff: ??? mV
WF: Verify LCD backlight current!



SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

PAGE TITLE
Voltage & Current Sensing

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

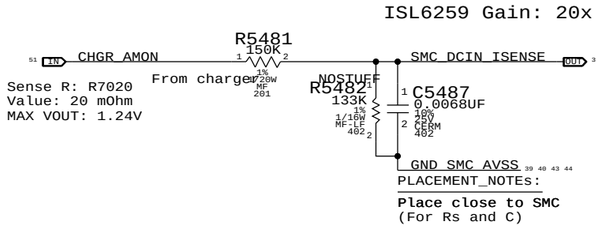
BRANCH

PAGE 53 OF 110

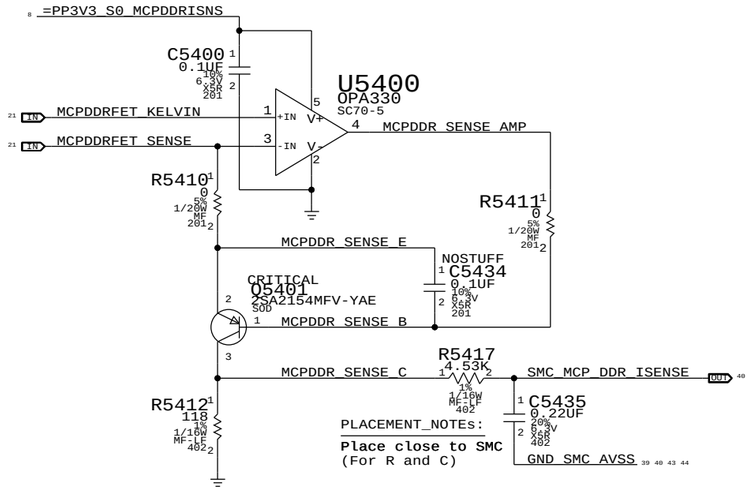
SHEET 43 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

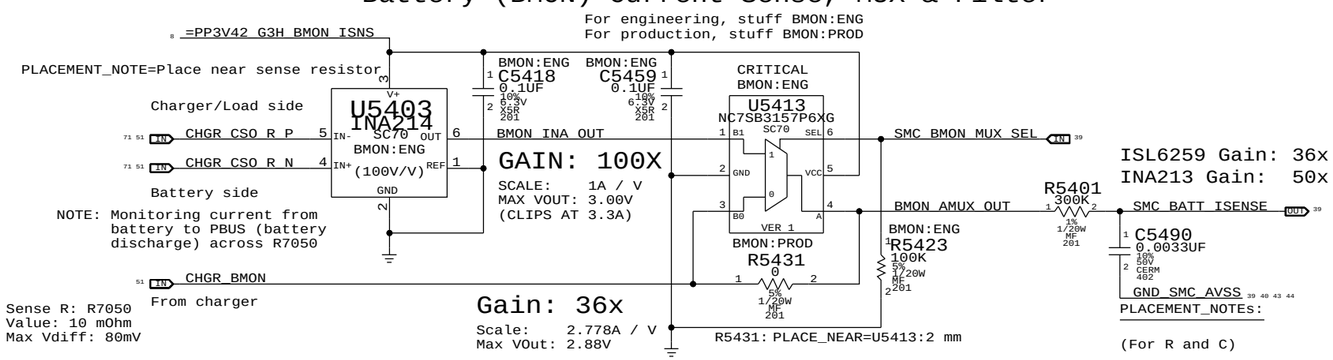
DCIN (AMON) Current Sense, RMUX & Filter



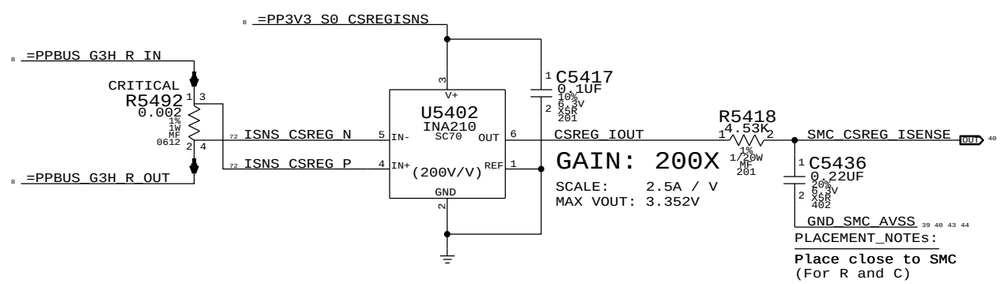
MCP MEM VDD Current Sense / Filter



Battery (BMON) Current Sense, MUX & Filter

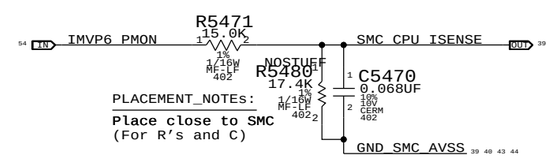


Chipset Regulators High-Side Current Sense / Filter

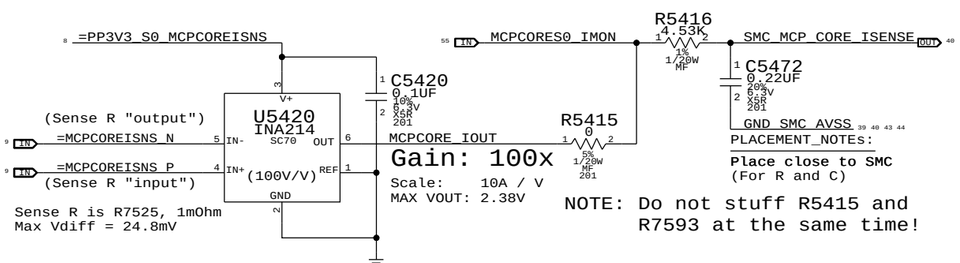


VERIFY ALL RESISTOR AND GAINS

CPU VCore Load Side Current Sense / Filter

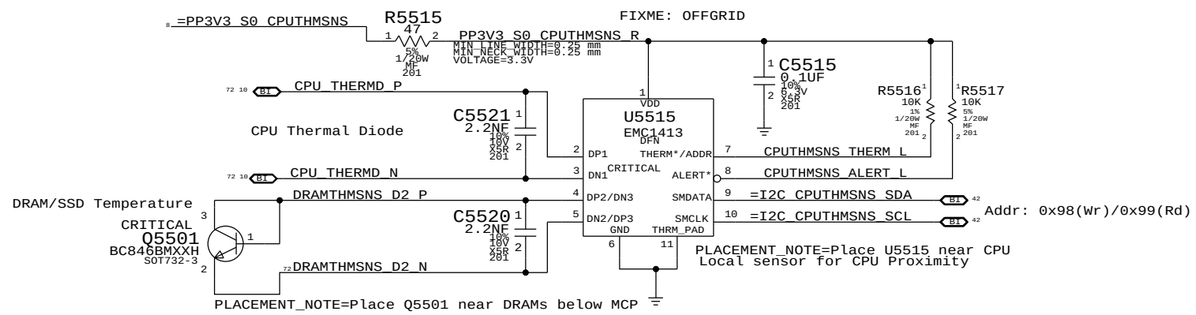


MCP VCore Current Sense Filter

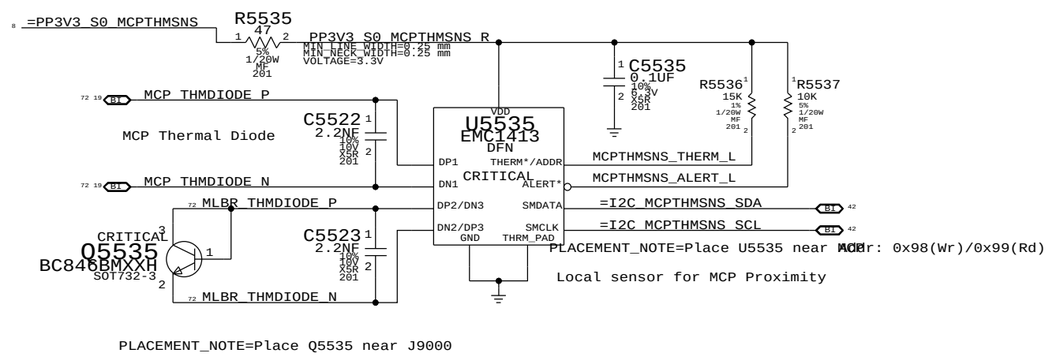


SYNC_MASTER=K99_MLB	SYNC_DATE=04/08/2010
PAGE TITLE: Current Sensing	
Apple Inc.	DRAWING NUMBER: 051-8467 / SIZE: D
	REVISION: 3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH
	PAGE: 54 OF 110
	SHEET: 44 OF 74

CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

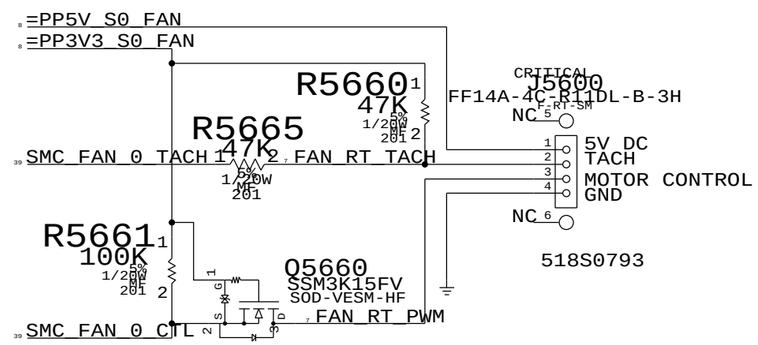
BRANCH

PAGE 55 OF 110

SHEET 45 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

FAN CONNECTOR



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
Fan

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

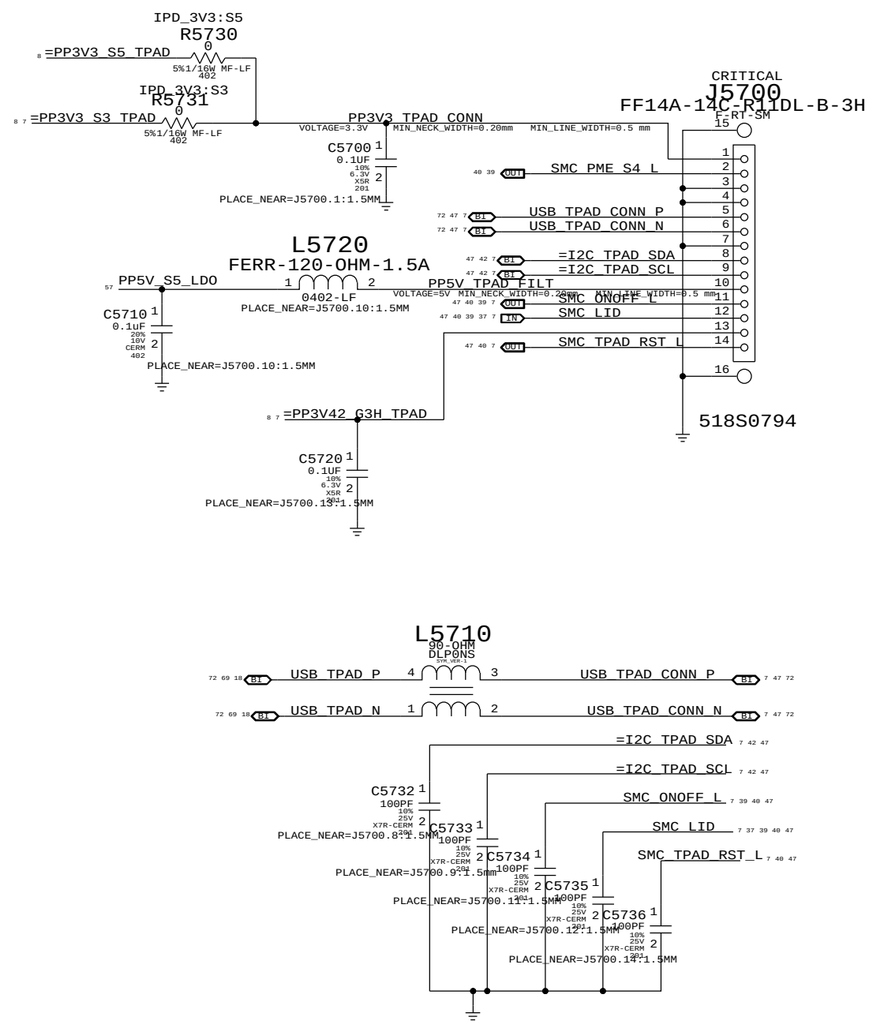
BRANCH

PAGE 56 OF 110

SHEET 46 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

IPD Flex Connector



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE

WELLSPRING 1

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

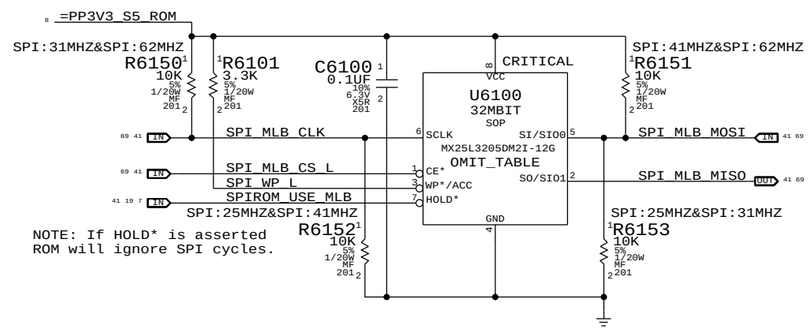
BRANCH

PAGE 57 OF 110

SHEET 47 OF 74

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.

MCP89 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 MHz use FAST_READ command.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
SPI ROM

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

PAGE 61 OF 110

SHEET 48 OF 74

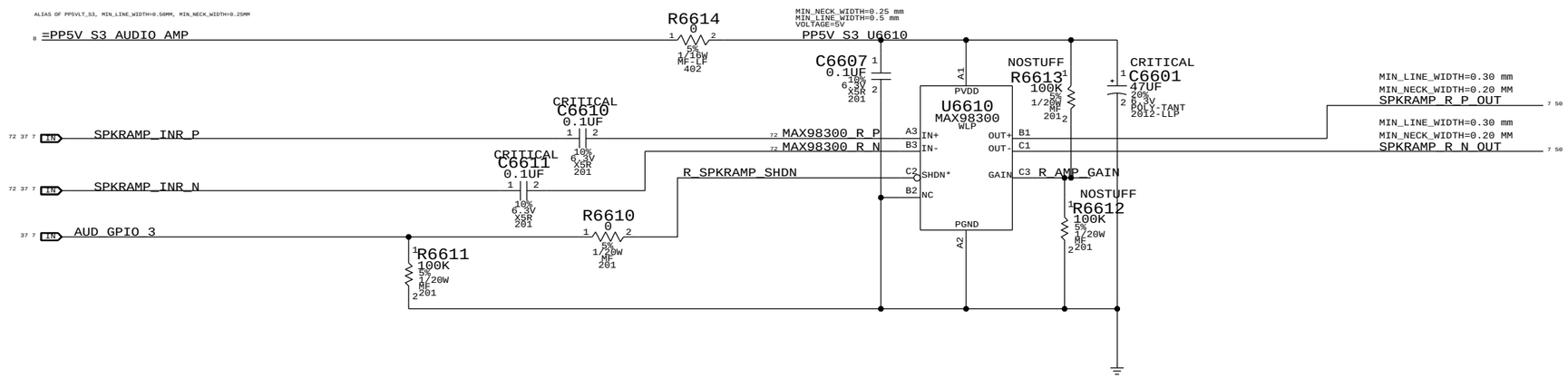
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

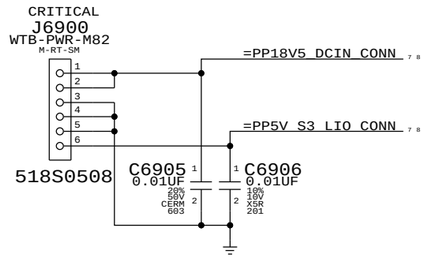
PAGE 66 OF 110

SHEET 49 OF 74

NOTICE OF PROPRIETARY PROPERTY:

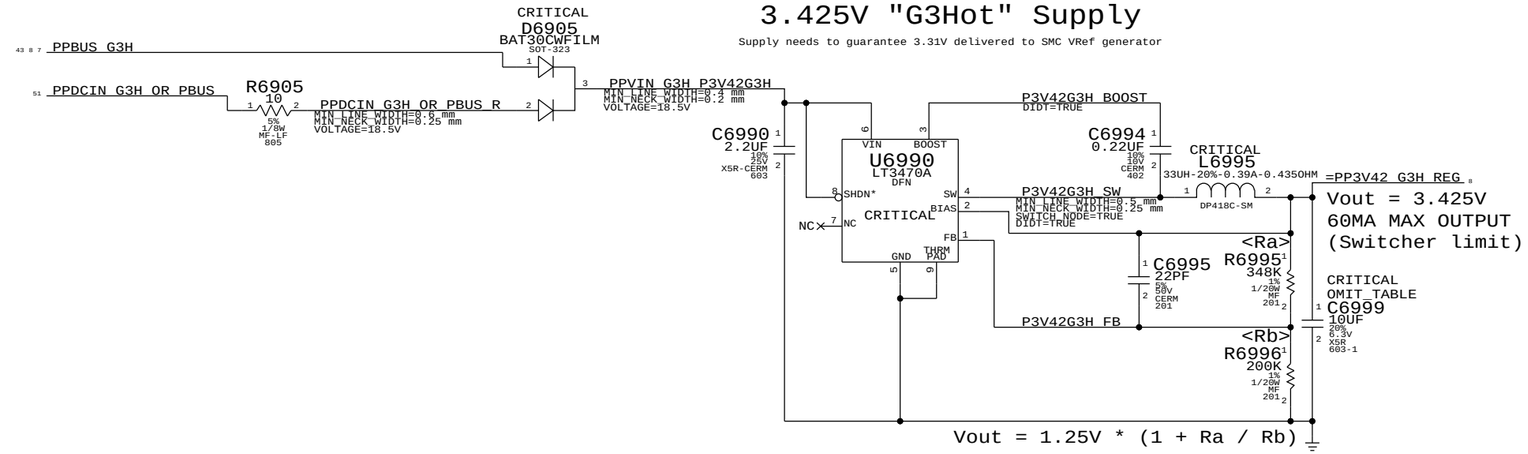
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

MLB to LIO Power Cable Connector



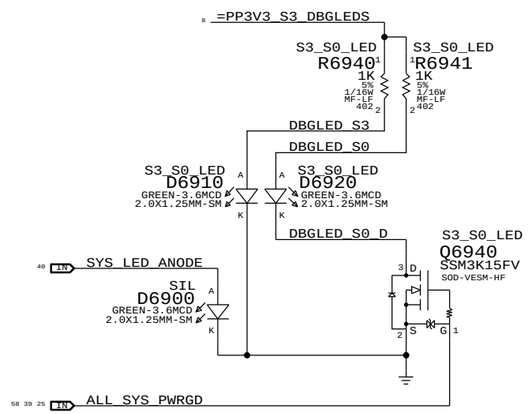
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

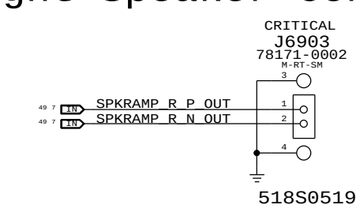


Debug LEDs

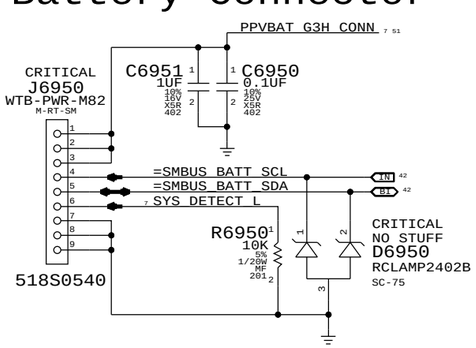
(For development only)



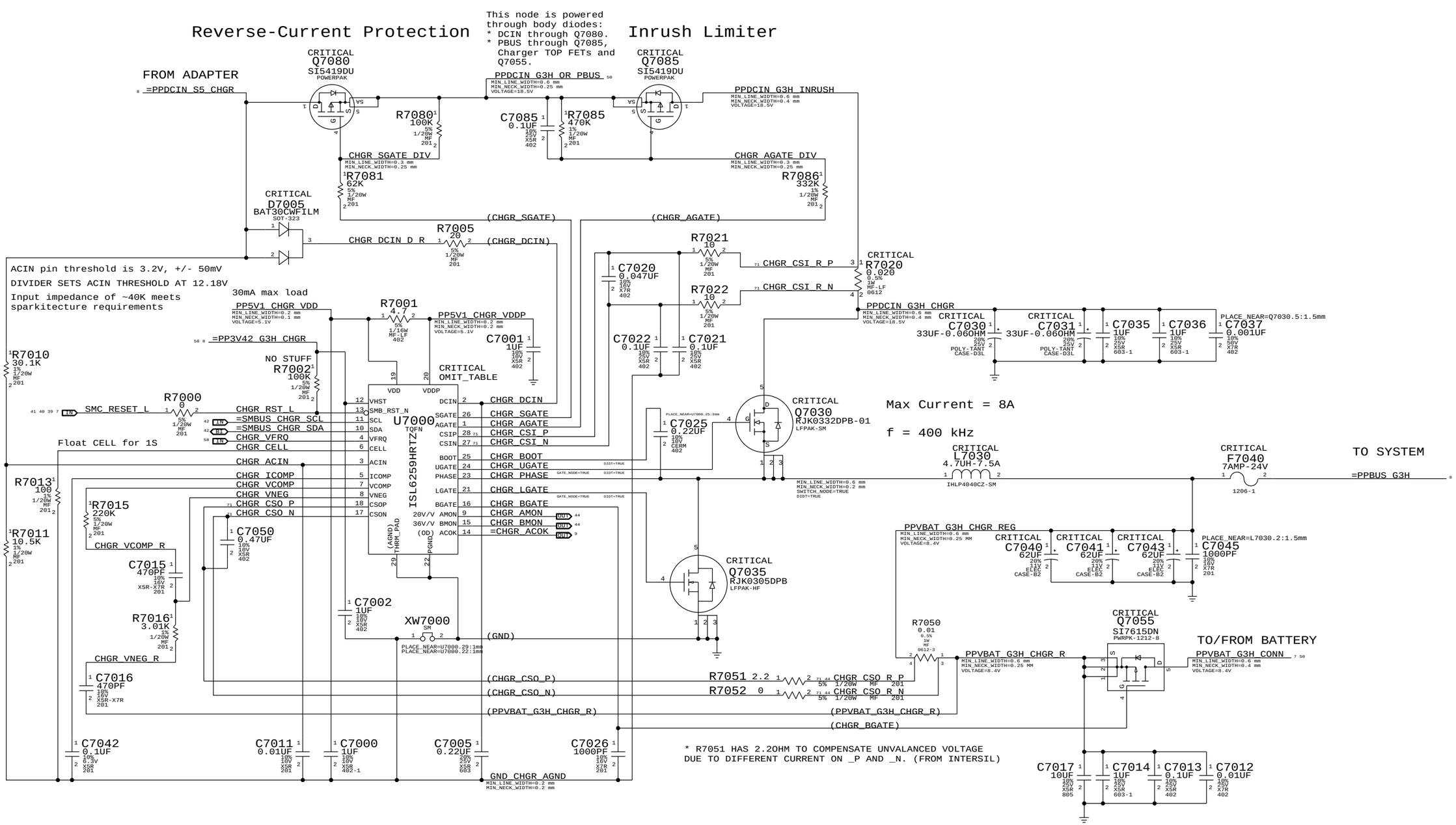
Right Speaker Connector



K16-Specific Battery Connector



SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
PAGE TITLE: DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER: 051-8467 — SIZE: D
	REVISION: 3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH
	PAGE: 69 OF 110
	SHEET: 50 OF 74



SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/16/2010)

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

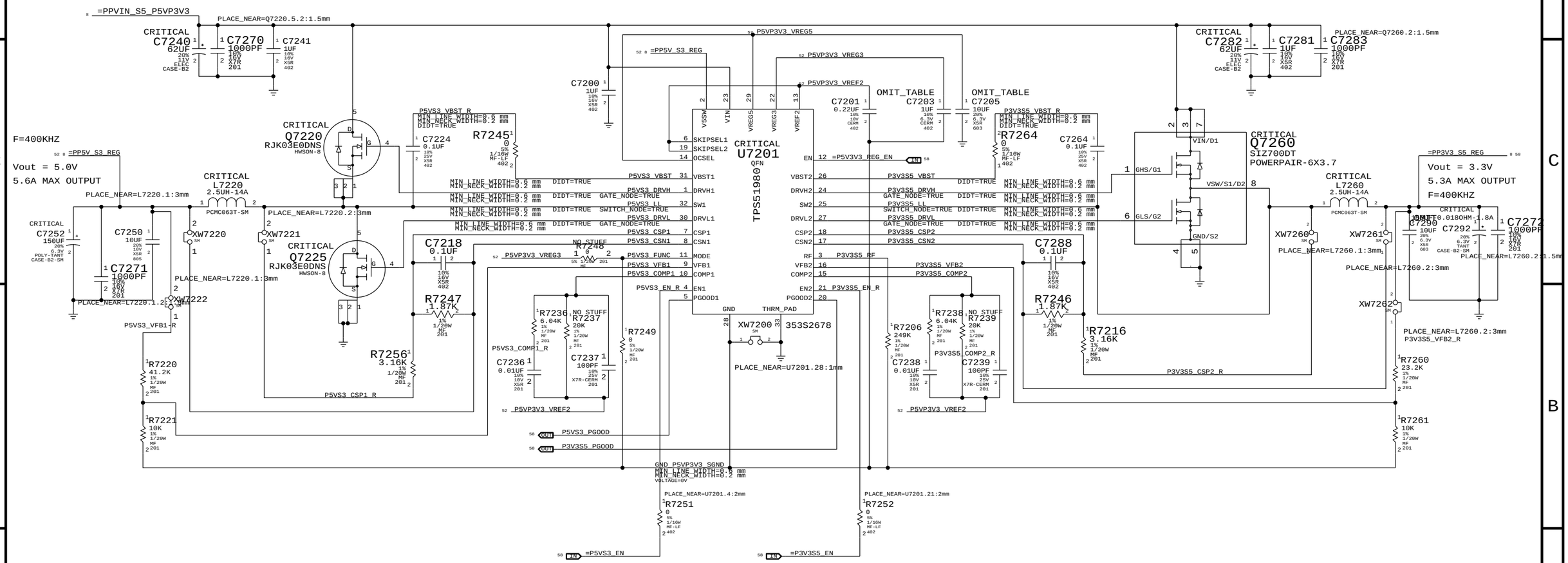
REVISION 3.3.0

BRANCH

PAGE 70 OF 110

SHEET 51 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

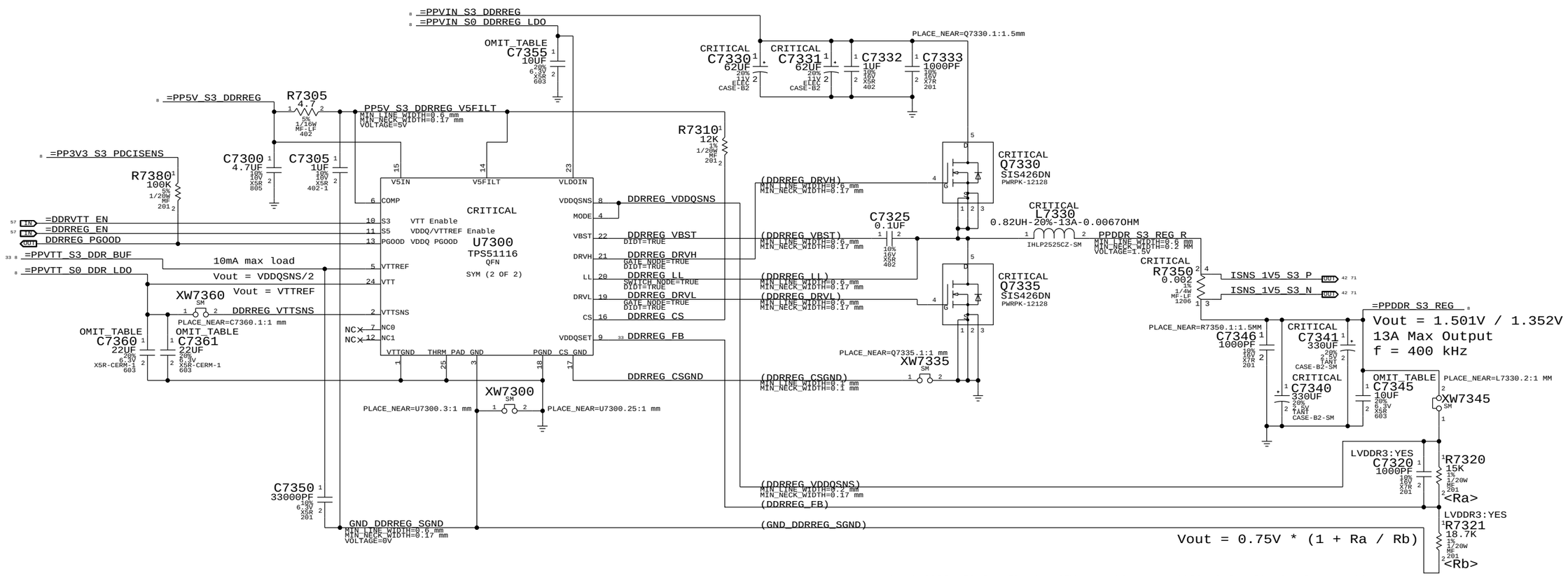
REVISION 3.3.0

BRANCH

PAGE 72 OF 110

SHEET 52 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



Use LVDDR3:YES for fixed 1.35V operation or LVDDR3:NO for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321		LVDDR3:NO

SYNC MASTER=K16_MLB SYNC DATE=06/01/2010

PAGE TITLE
1.5V/1.35V LVDDR3 Supply

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

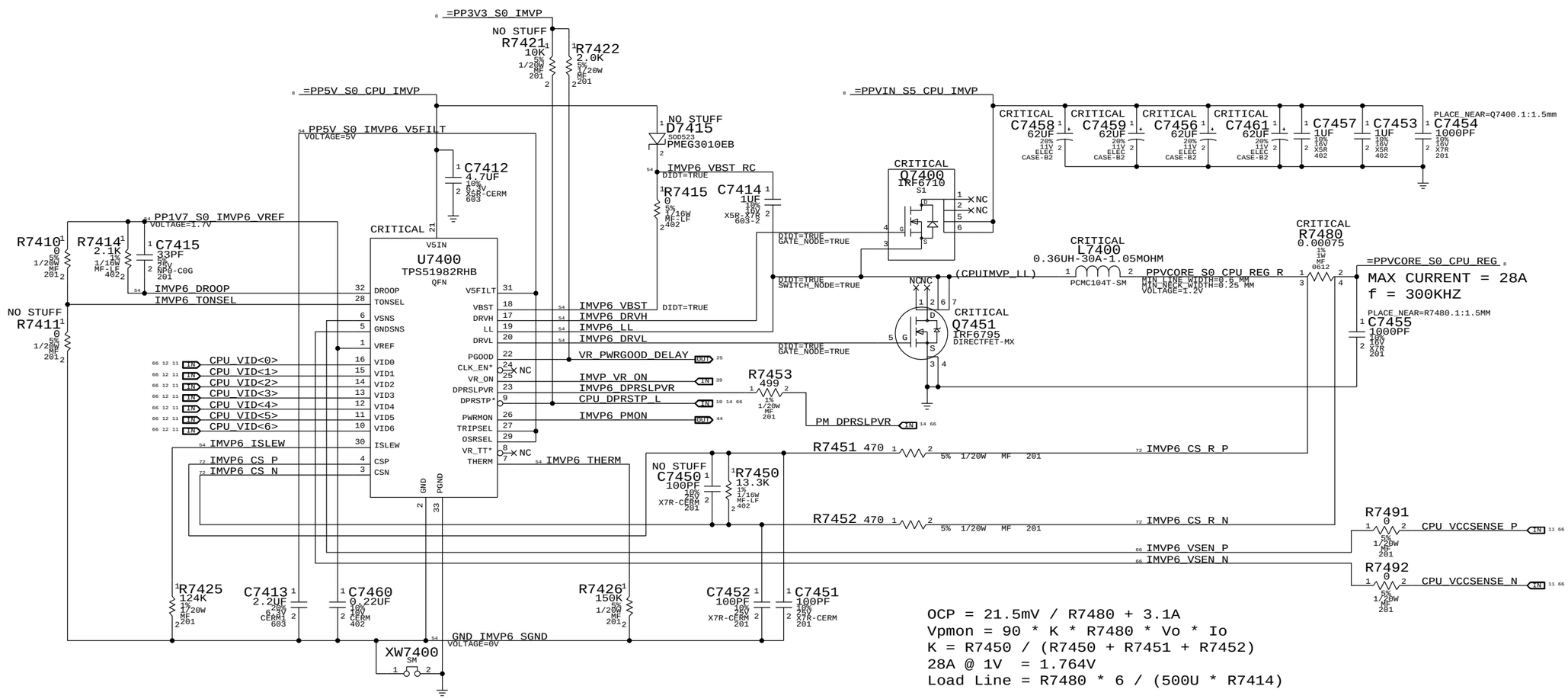
REVISION 3.3.0

BRANCH

PAGE 73 OF 110

SHEET 53 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



OCP = 21.5mV / R7480 + 3.1A
Vpmon = 90 * K * R7480 * Vo * Io
K = R7450 / (R7450 + R7451 + R7452)
28A @ 1V = 1.764V
Load Line = R7480 * 6 / (500U * R7414)

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_THERM	0.25 MM	0.20 MM
IMVP6_ISLEW	0.25 MM	0.20 MM
PP1V7_S0_IMVP6_VREF	0.25 MM	0.20 MM
PP5V_S0_IMVP6_V5FILT	0.25 MM	0.20 MM
IMVP6_LL	1.5 MM	0.20 MM
IMVP6_VBST	0.25 MM	0.20 MM
IMVP6_DRVH	1.5 MM	0.20 MM
IMVP6_DRVL	1.5 MM	0.20 MM
IMVP6_VBST_RC	1.5 MM	0.20 MM

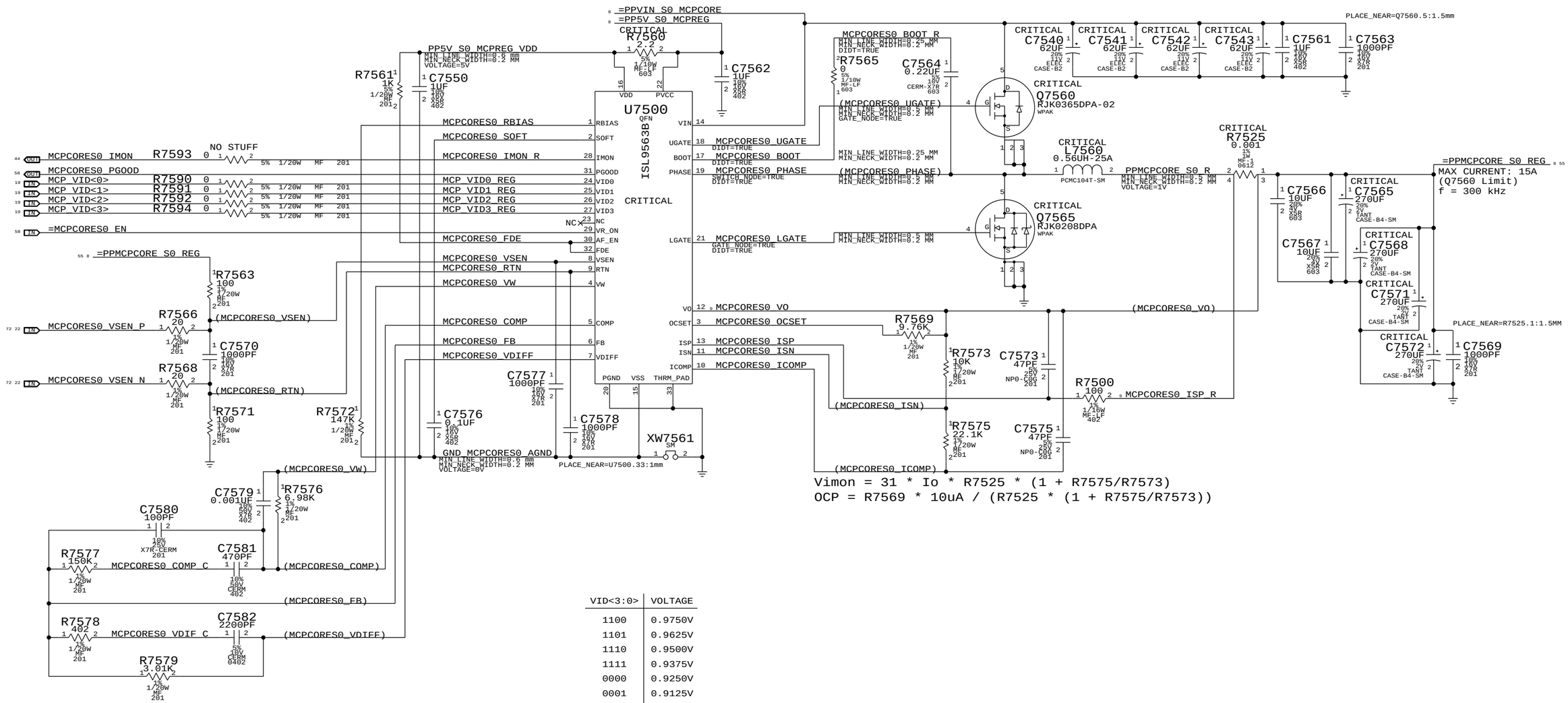
SYNC MASTER=(K99_MLB) SYNC DATE=(02/16/2010)

PAGE TITLE
IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 74 OF 110
SHEET 54 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



Vimon = 31 * Io * R7525 * (1 + R7575/R7573)
OCP = R7569 * 10uA / (R7525 * (1 + R7575/R7573))

VID<3:0>	VOLTAGE
1100	0.9750V
1101	0.9625V
1110	0.9500V
1111	0.9375V
0000	0.9250V
0001	0.9125V
0010	0.9000V
0011	0.8875V
0100	0.8750V
0101	0.8625V
0110	0.8500V
0111	0.8375V
1000	0.8250V
1001	0.8125V
1010	0.8000V
1011	0.7875V

K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

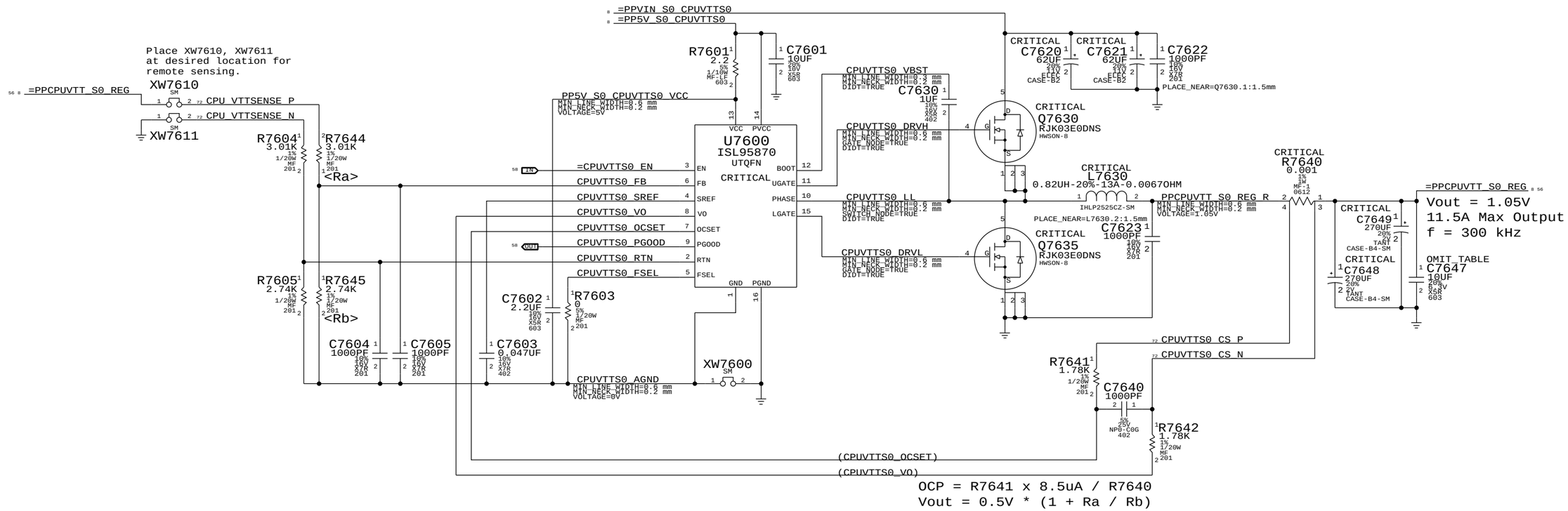
SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/11/2010)

PAGE TITLE
MCP VCore Regulator

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 75 OF 110
SHEET 55 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=(K99_MLB) SYNC_DATE=(03/01/2010)

PAGE TITLE
CPUVTT (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

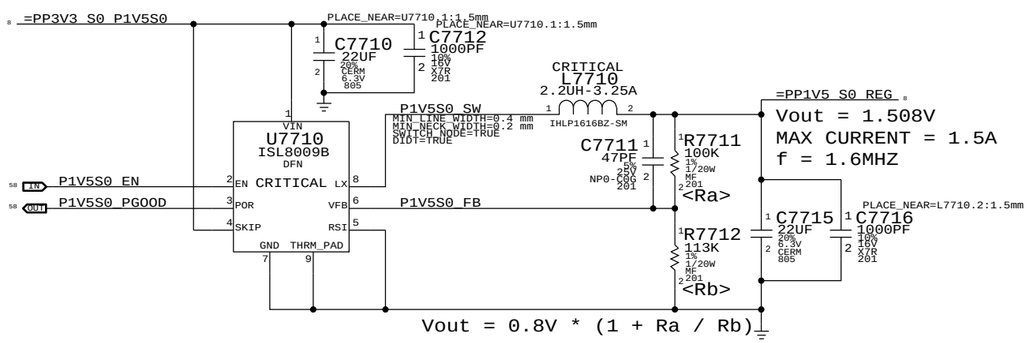
BRANCH

PAGE 76 OF 110

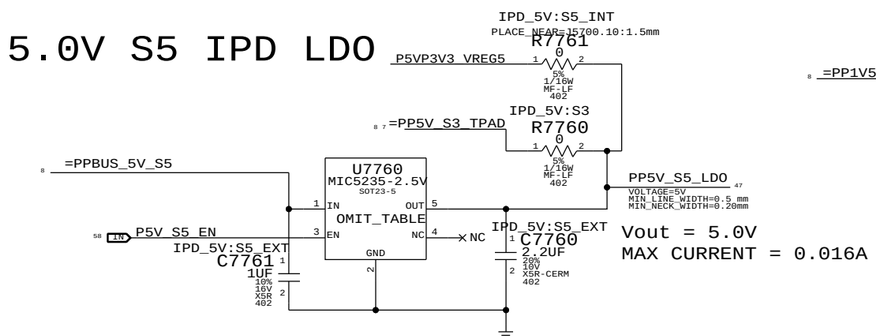
SHEET 56 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

1.5V S0 Regulator

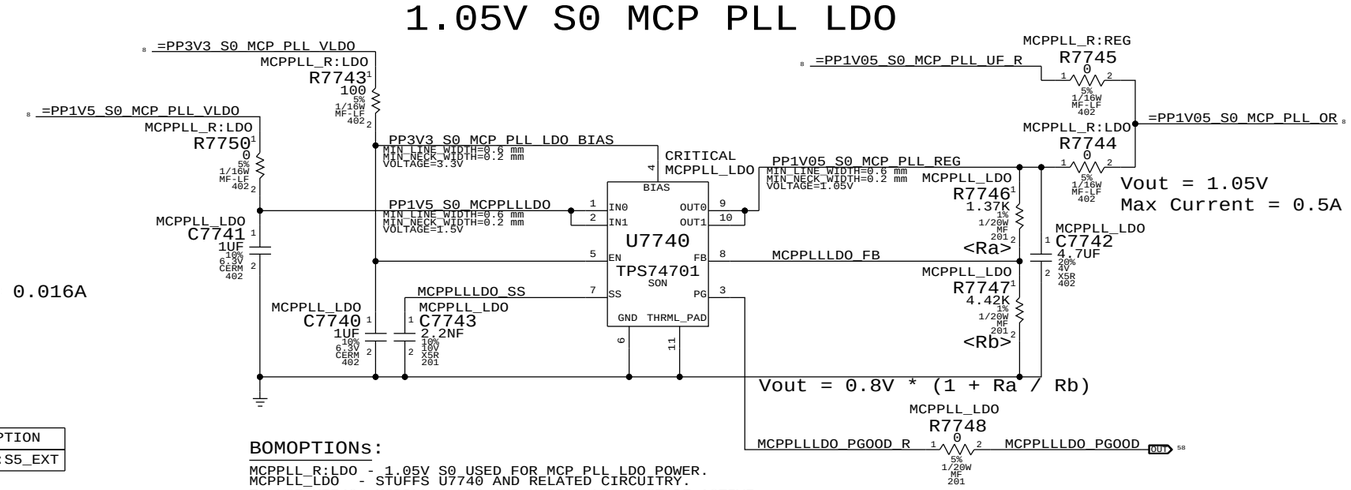


5.0V S5 IPD LDO



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3034	1	IC,LDO,MIC5235,5V,1%,150MA,SOT23-5	U7760		IPD_5V:S5_EXT

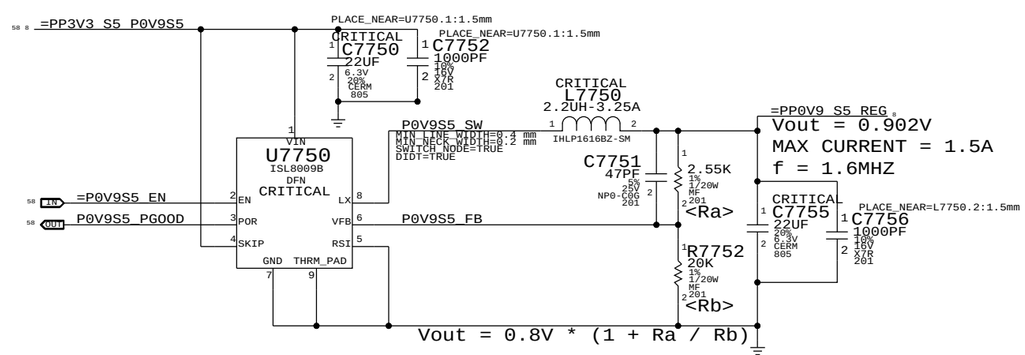
1.05V S0 MCP PLL LDO



BOMOPTIONs:

MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

MCP 0.9V S5 (AUXC) Switcher



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

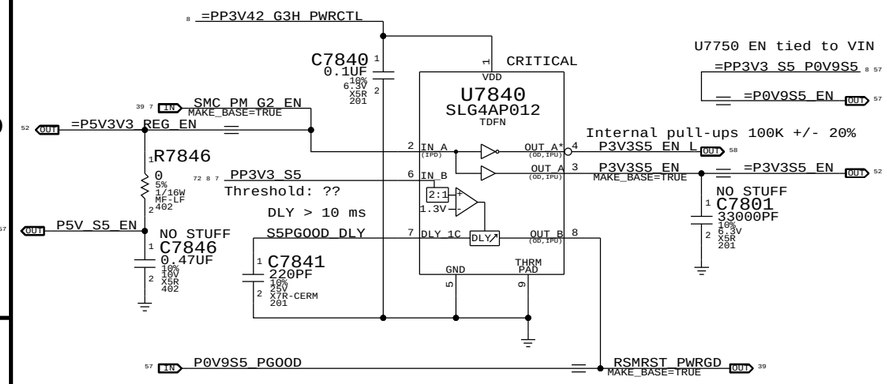
BRANCH:

PAGE: 77 OF 110

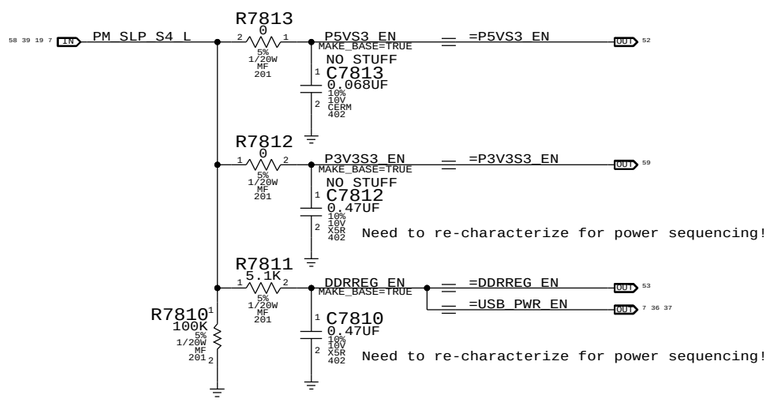
SHEET: 57 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

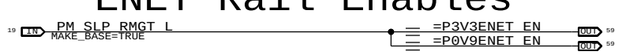
S5 Rail Enables & PGOOD



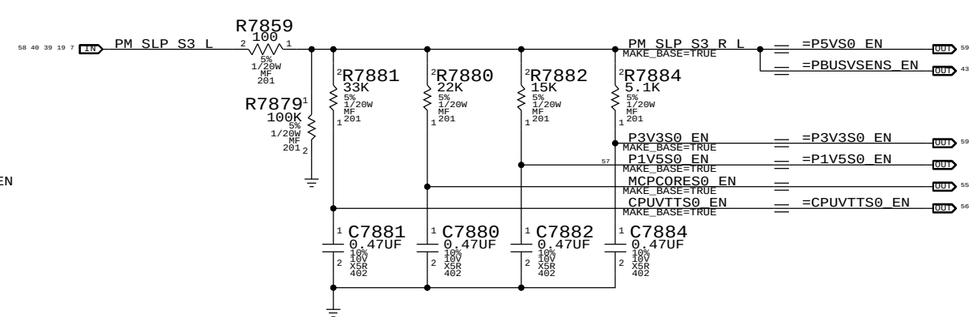
S3 Rail Enables



ENET Rail Enables



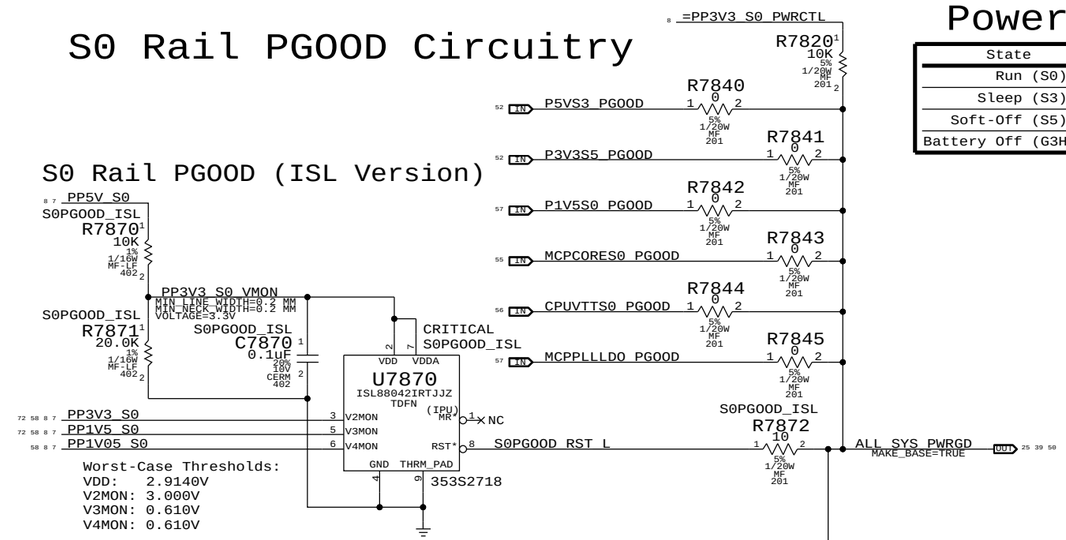
S0 Rail Enables



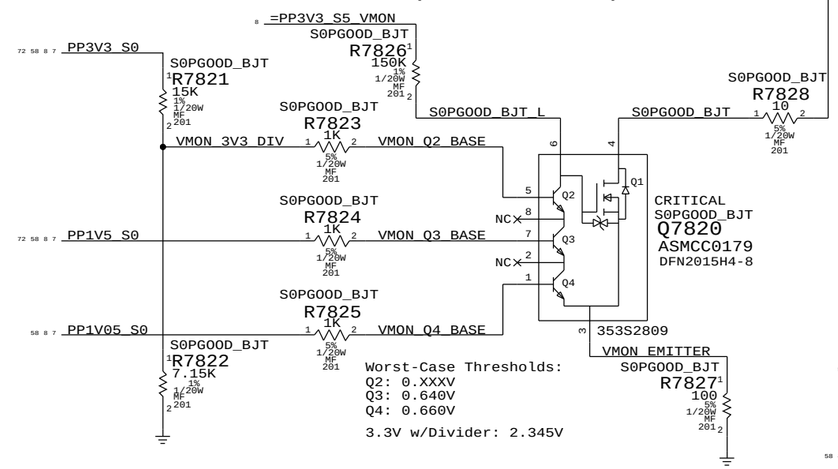
VTT Rail Enable

VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

S0 Rail PGOOD Circuitry



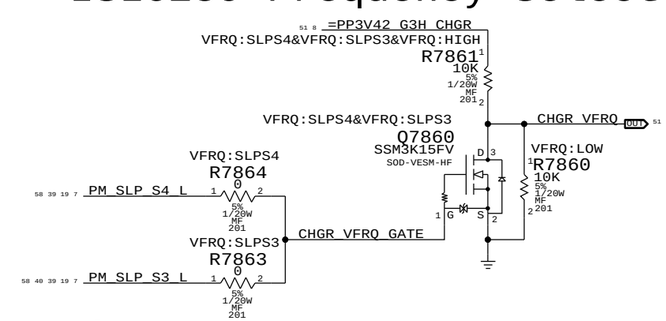
S0 Rail PGOOD (BJT Version)



Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

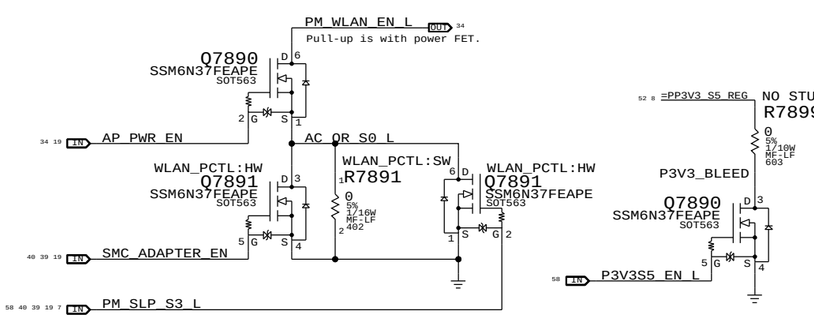
ISL6259 Frequency Select



WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.
NOTE: "AC" term valid only when Q7891 is stuffed



SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE: Power Sequencing

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

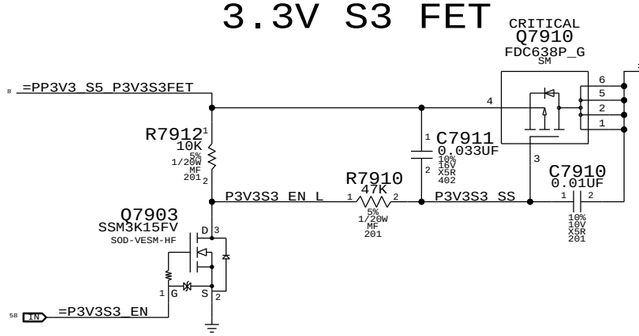
BRANCH

PAGE: 78 OF 110

SHEET: 58 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

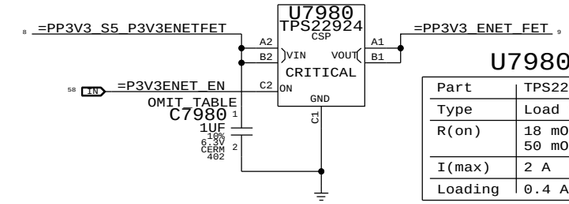
3.3V S3 FET



Q7910

MOSFET	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	1.274 A (EDP)

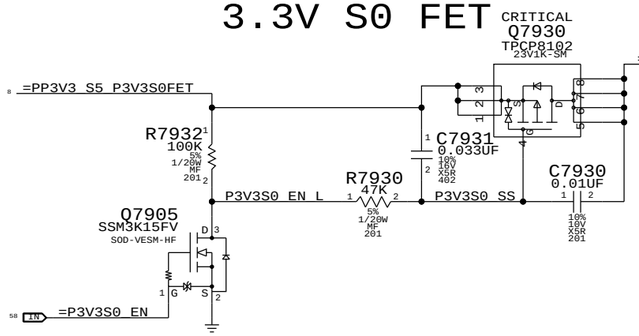
3.3V ENET Switch



U7980

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max
I(max)	2 A
Loading	0.4 A (EDP)

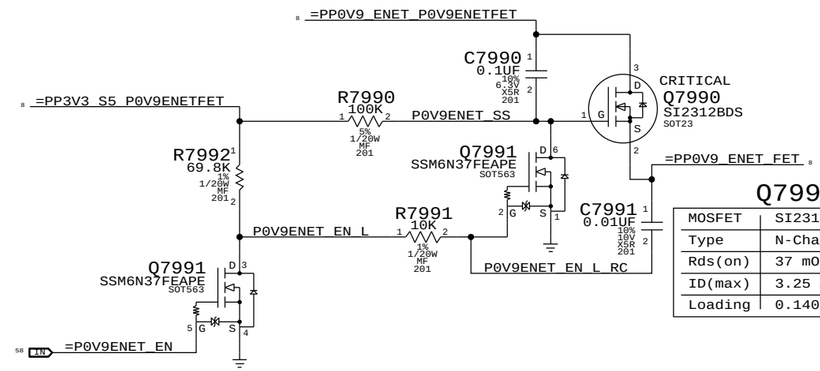
3.3V S0 FET



Q7930

MOSFET	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
ID(max)	7.2 A @85C
Loading	3.294 A (EDP)

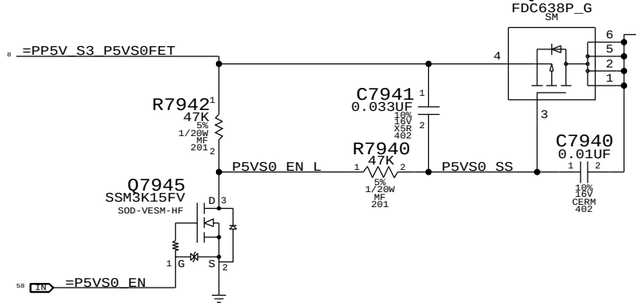
0.9V ENET FET



Q7990

MOSFET	SI2312BDS
Type	N-Channel
Rds(on)	37 mOhm @2.5V
ID(max)	3.25 A @85C
Loading	0.140 A (EDP)

5V S0 FET



Q7940

Part	FDC638P
Type	P-Channel
Rds(on)	65 mOhm @2.5V
ID(max)	2.0 A @85C
Loading	0.100 A (EDP)

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
Power FETs

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

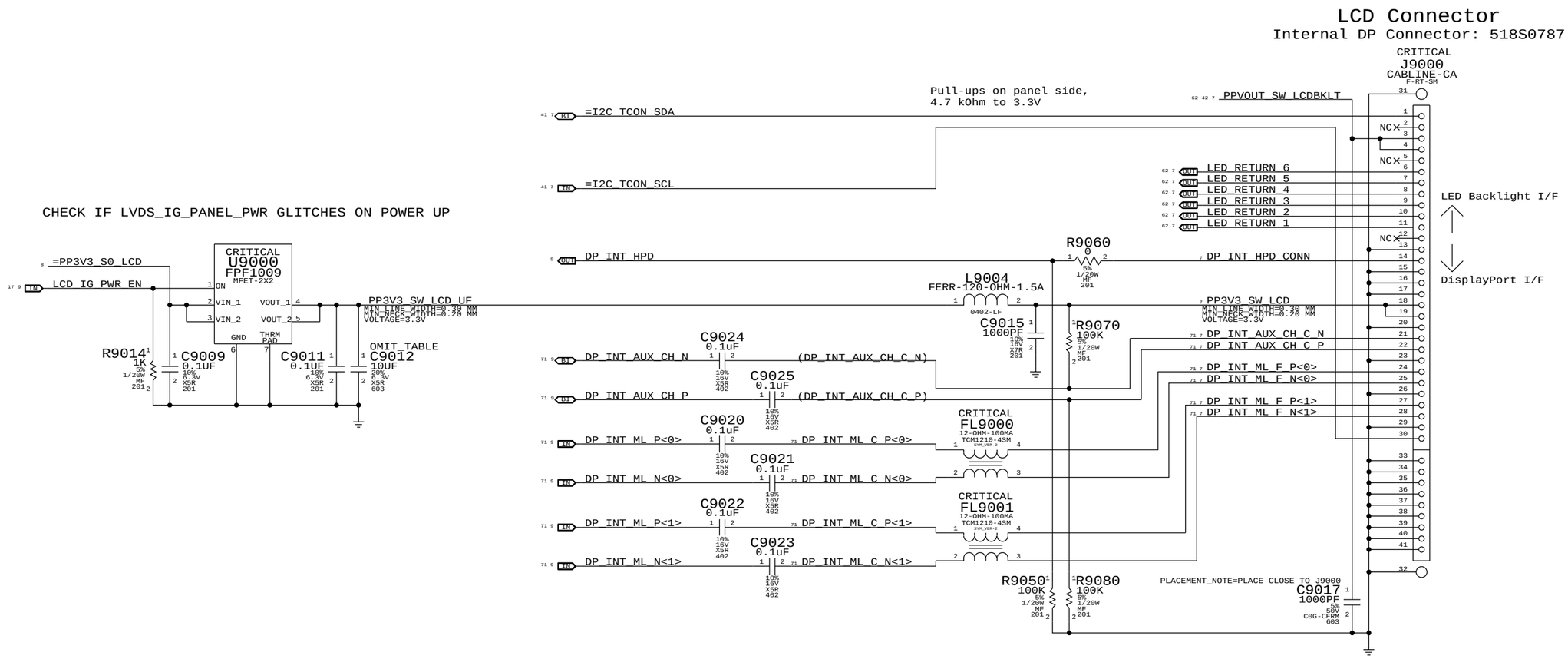
REVISION 3.3.0

BRANCH

PAGE 79 OF 110

SHEET 59 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=K99_MLB SYNC_DATE=07/23/2010

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

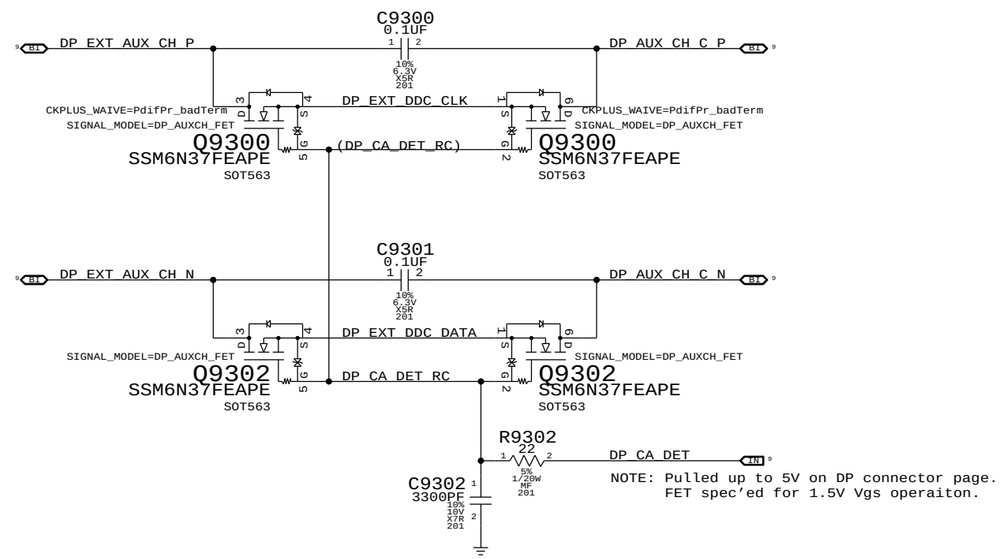
REVISION 3.3.0

BRANCH

PAGE 90 OF 110

SHEET 60 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



NOTE: Pulled up to 5V on DP connector page.
FET spec'ed for 1.5V Vgs operaiton.

SYNC MASTER=K99 MLB SYNC DATE=04/08/2010

PAGE TITLE
External DisplayPort Support

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

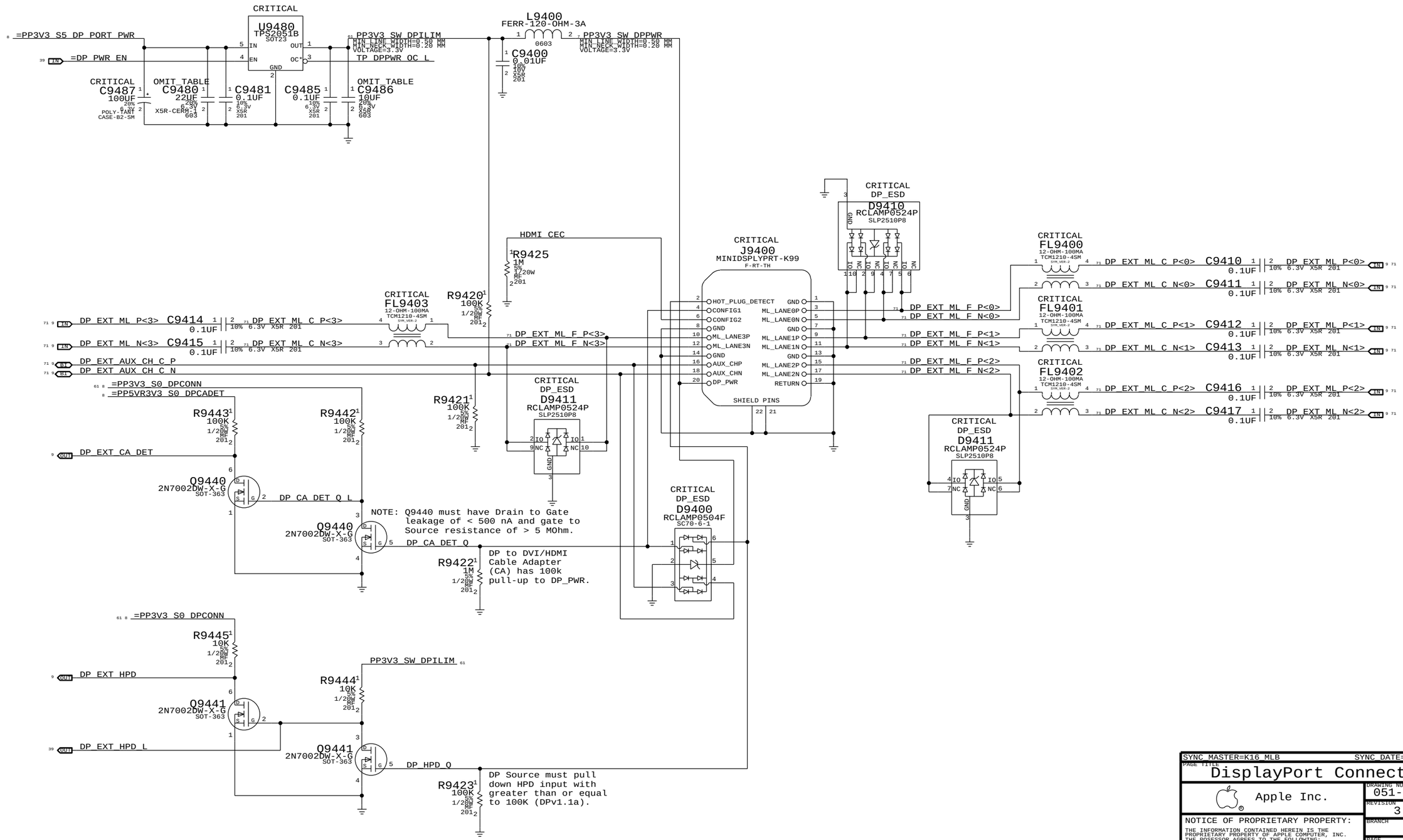
BRANCH

PAGE 93 OF 110

SHEET 61 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Port Power Switch



SYNC_MASTER=K16_MLB SYNC_DATE=06/01/2010

PAGE TITLE
DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

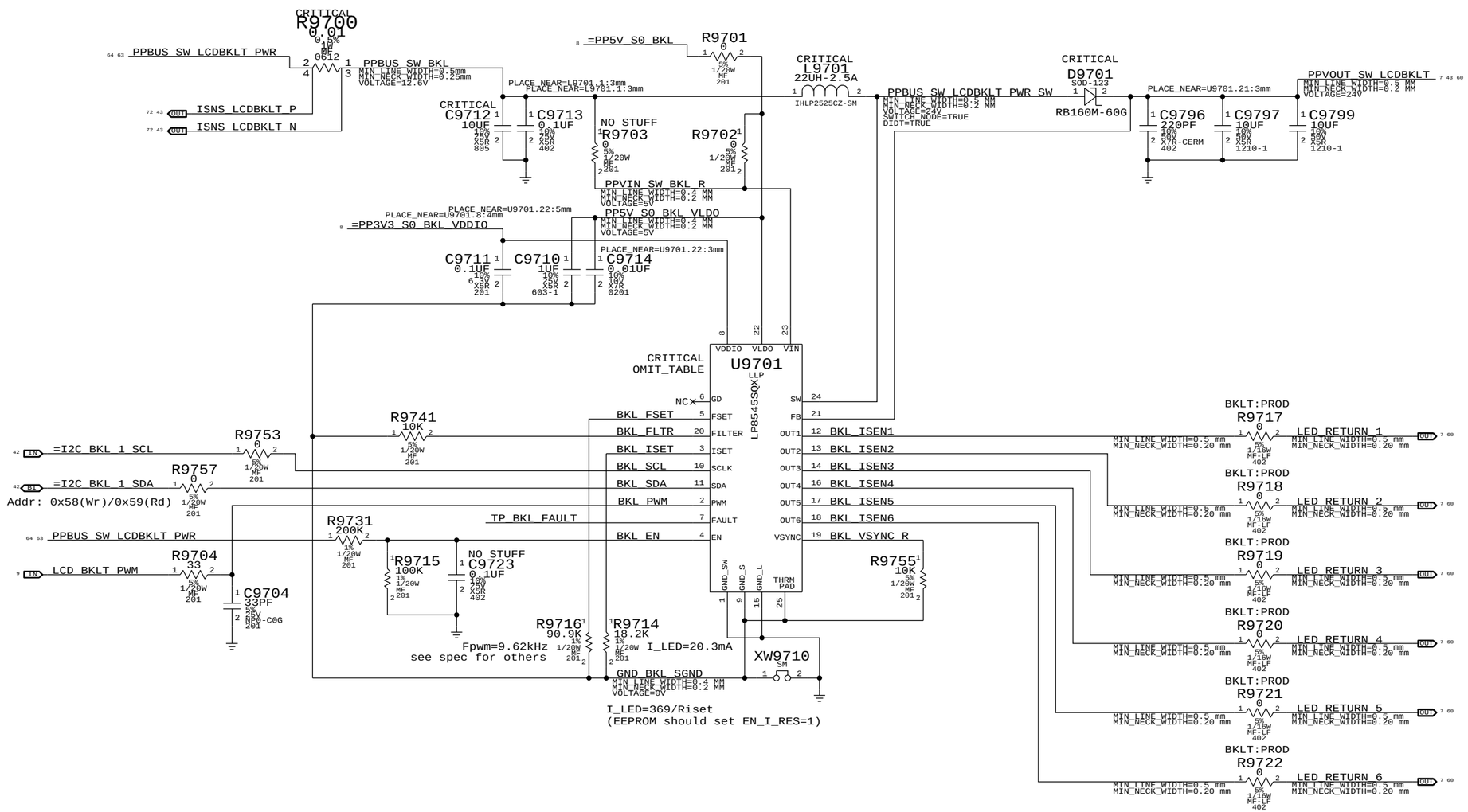
BRANCH

PAGE 94 OF 110

SHEET 62 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



FOR LP8543:
STUFF R9741
NO STUFF R9740, C9740, C9741, R9754

PART NUMBER	QTY		REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
353S2896	1	IC,LP8545,LED BKLT CTRLR,PRODUCTIO,LLP24	U9701	CRITICAL	PROJ:K16
353S2967	1	IC,LP8545,LED BKLT CTRLR,LLP24,K99 VER	U9701	CRITICAL	PROJ:K99

10.2 ohm resistors for current measurement on LED strings.

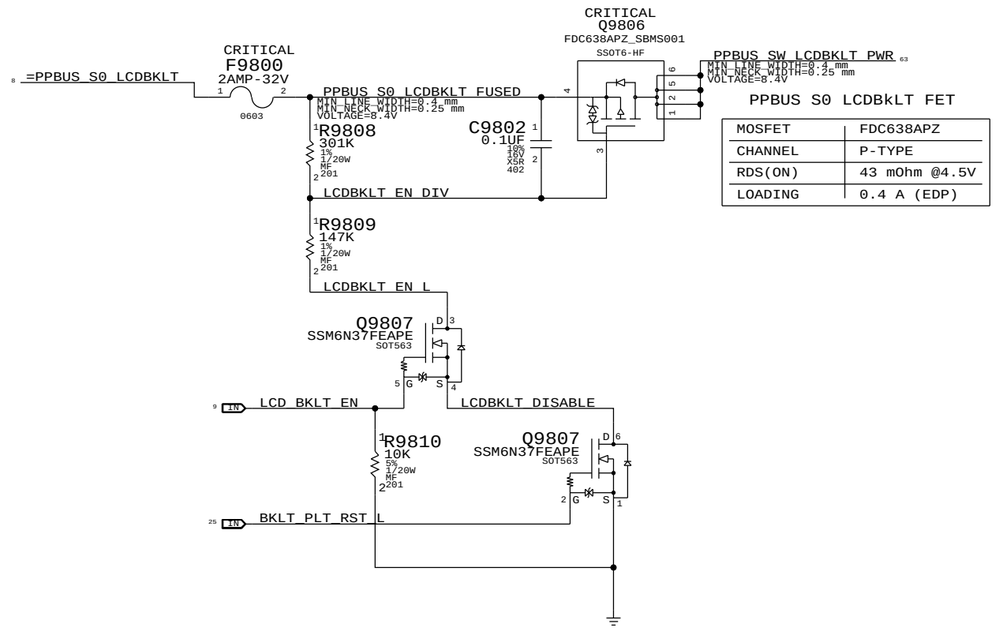
SYNC MASTER=(K99 MLB) SYNC DATE=(03/01/2010)

PAGE TITLE
LCD Backlight Driver

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 97 OF 110
SHEET 63 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
LCD Backlight Support

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

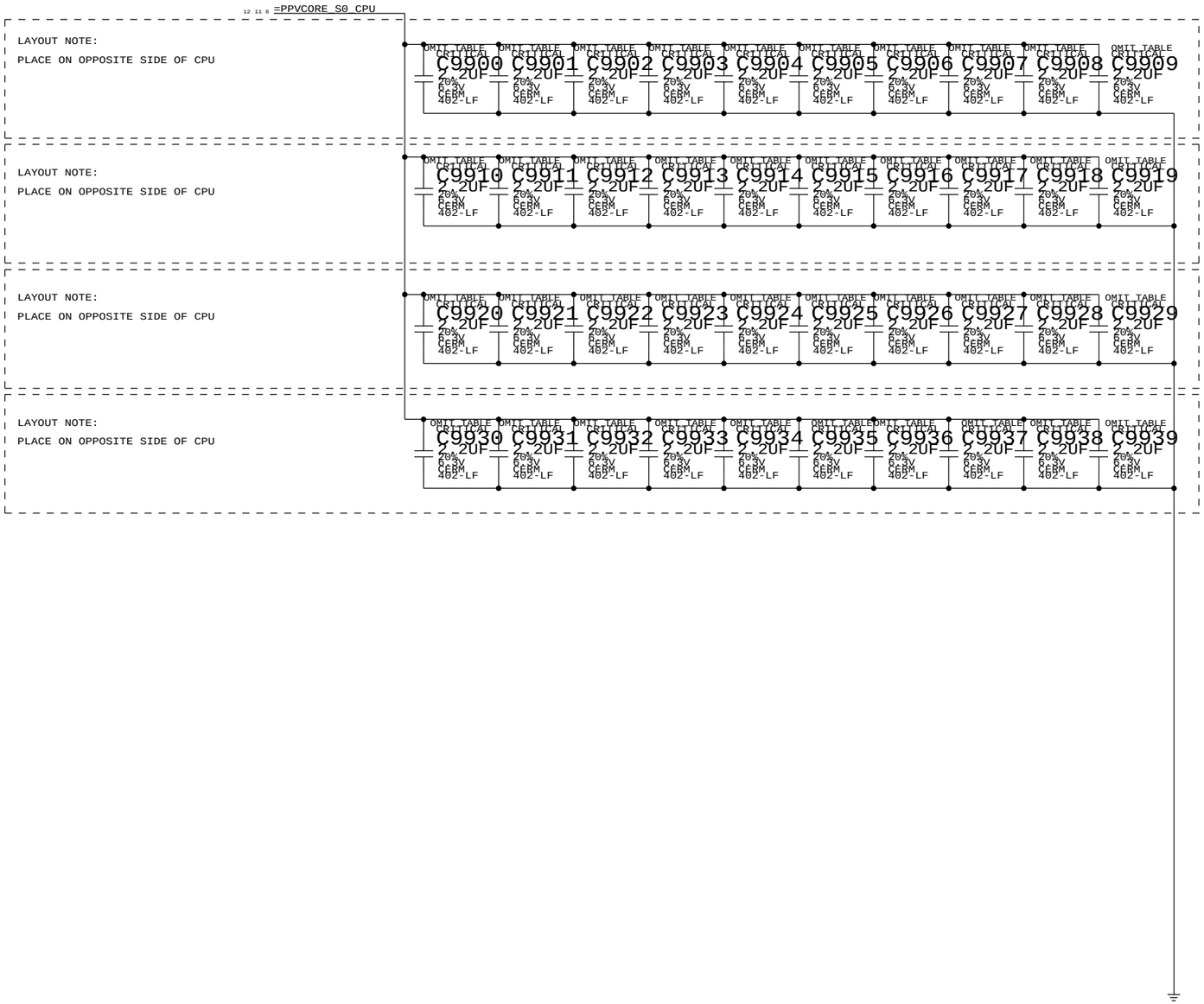
PAGE 98 OF 110

SHEET 64 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

ADDITIONAL CPU VCORE HF DECOUPLING

40x 1uF 0402



SYNC_MASTER=K99_MLB SYNC_DATE=05/18/2010

PAGE TITLE
Additional CPU/GPU Decoupling

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

PAGE 99 OF 110

SHEET 65 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
	FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_55S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_55S	FSB_1X	FSB_BREQ0_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_55S	FSB_1X	FSB_CPURST_L	10 13 14
	FSB_1X	FSB_55S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_55S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_55S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_55S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_55S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU_INTR	10 14
	CPU_ASYNC_R	CPU_55S	CPU_AGTL	CPU_NMI	10 14
	CPU_PROCHOT_L	CPU_55S	CPU_AGTL	CPU_PROCHOT_L	10 14 40
	CPU_PWRGD	CPU_55S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_55S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_55S	CPU_8MIL	PM_THRMTRIP_L	10 14 40
	FSB_CPUSLP_L	CPU_55S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_55S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_55S	CPU_AGTL	CPU_DPRSTP_L	10 14 54
	CPU_ASYNC	CPU_55S	CPU_AGTL	FSB_DPWR_L	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_55S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_55S	CPU_AGTL	PM_DPRSLPVR	14 54
	(See above)	CPU_55S	CPU_AGTL	IMVP_DPRSLPVR	
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 33
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
	XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
	XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
	XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
	XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
	XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP_CPURST_L	13
		CPU_55S	CPU_8MIL	CPU_VID<6..0>	11 12 54
		CPU_55S	CPU_8MIL	IMVP6_VID<6..0>	12
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 54
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 54
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	54
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	54

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
CPU/FSB Constraints

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 100 OF 110
SHEET 66 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
MEM_CLK2MEM	*	=4:1_SPACING	?	NV DG says 3x inner, 4x outer
MEM_CTRL2CTRL	*	=2:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CTRL2MEM	*	=2.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2CMD	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_CMD2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2DATA	*	=1.5:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DATA2MEM	*	=3:1_SPACING	?	NV DG says 2x inner, 4x outer
MEM_DQS2MEM	*	=3:1_SPACING	?	NV DG says 4x inner, 5x outer
MEM_2OTHER	*	25 MIL	?	

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 360 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
CMD/CTRL signals should be matched within 150 ps.
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_P<5..0>	9 15 26 27 32
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_A_CLK_N<5..0>	9 15 26 27 32
MEM_A_CKE	MEM_50S	MEM_CTRL	MEM_A_CKE<3..0>	15 21 26 27 32
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_CS_L<3..0>	15 26 27 32
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_ODT<3..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_A<15..0>	9 15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_BA<2..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_RAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_CAS_L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_WE_L	15 26 27 32
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DM<0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DM<1>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DM<2>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DM<3>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DM<7>	15 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 26
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 26
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 26
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 26
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 26
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_P<5..0>	9 15 28 29 32
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_B_CLK_N<5..0>	9 15 28 29 32
MEM_B_CKE	MEM_50S	MEM_CTRL	MEM_B_CKE<3..0>	15 21 28 29 32
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_CS_L<3..0>	15 28 29 32
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_ODT<3..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_A<15..0>	9 15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_BA<2..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_RAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_CAS_L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_WE_L	15 28 29 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	15

SYNC MASTER=K99_MLB SYNC DATE=04/08/2010

PAGE TITLE
Memory Constraints

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 101 OF 110
SHEET 67 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	
	PCIE_90D	PCIE	PCIE_AP_R2D_P	7 34
	PCIE_90D	PCIE	PCIE_AP_R2D_N	7 34
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE_AP_R2D_C_P	16 34
	PCIE_90D	PCIE	PCIE_AP_R2D_C_N	16 34
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE_AP_D2R_P	7 16 34
	PCIE_90D	PCIE	PCIE_AP_D2R_N	7 16 34
	PCIE_90D	PCIE	PCIE_ENET_R2D_P	
	PCIE_90D	PCIE	PCIE_ENET_R2D_N	
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE_ENET_R2D_C_P	
	PCIE_90D	PCIE	PCIE_ENET_R2D_C_N	
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE_ENET_D2R_P	
	PCIE_90D	PCIE	PCIE_ENET_D2R_N	
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_P	
	PCIE_90D	PCIE	PCIE_ENET_D2R_C_N	
	PCIE_90D	PCIE	PCIE_FW_R2D_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_N	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	9 16
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	9 16
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_P	7 16 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_AP_N	7 16 34
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX0_TERMP	16
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	
DP_INT_ML	DP_90D	DISPLAYPORT	DP_IG_ML1_P<1..0>	9 17
DP_INT_ML	DP_90D	DISPLAYPORT	DP_IG_ML1_N<1..0>	9 17
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH1_P	9 17
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH1_N	9 17
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML0_P<3..0>	9 17
DP_EXT_ML	DP_90D	DISPLAYPORT	DP_IG_ML0_N<3..0>	9 17
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH0_P	9 17
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP_IG_AUX_CH0_N	9 17
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET	17 24
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE	17 24
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17 24
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17 24
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	18 35
	SATA_90D	SATA	SATA_HDD_R2D_C_N	18 35
	SATA_90D	SATA	SATA_HDD_R2D_P	7 35
	SATA_90D	SATA	SATA_HDD_R2D_N	7 35
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	18 35
	SATA_90D	SATA	SATA_HDD_D2R_N	18 35
	SATA_90D	SATA	SATA_HDD_D2R_C_P	7 35
	SATA_90D	SATA	SATA_HDD_D2R_C_N	7 35
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	9 18
	SATA_90D	SATA	SATA_ODD_R2D_C_N	9 18
	SATA_90D	SATA	SATA_ODD_R2D_P	
	SATA_90D	SATA	SATA_ODD_R2D_N	
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	9 18
	SATA_90D	SATA	SATA_ODD_D2R_N	9 18
	SATA_90D	SATA	SATA_ODD_D2R_C_P	
	SATA_90D	SATA	SATA_ODD_D2R_C_N	
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	18

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
MCP Constraints 1

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D
REVISION 3.3.0
BRANCH
PAGE 102 OF 110
SHEET 68 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_55S	LPC	LPC AD<3..0>	7 19 39 41
LPC_FRAME_L	LPC_55S	LPC	LPC FRAME L	7 19 39 41
LPC_RESET_L	LPC_55S	LPC	LPC RESET L	19 25
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC R	19 25
	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	25 39
	CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	7 25 41
USB_EXTA	USB_90D	USB	USB EXTA P	18 36
	USB_90D	USB	USB EXTA N	18 36
	USB_90D	USB	USB EXTA MUXED P	36 72
	USB_90D	USB	USB EXTA MUXED N	36 72
USB_MINI	USB_90D	USB	USB MINI P	9 18
	USB_90D	USB	USB MINI N	9 18
USB_EXTD	USB_90D	USB	USB EXTD P	7 18 37
	USB_90D	USB	USB EXTD N	7 18 37
USB_CAMERA	USB_90D	USB	USB CAMERA P	7 18 37
	USB_90D	USB	USB CAMERA N	7 18 37
USB_BT	USB_90D	USB	USB BT P	7 18 34
	USB_90D	USB	USB BT N	7 18 34
USB_TPAD	USB_90D	USB	USB TPAD P	18 47 72
	USB_90D	USB	USB TPAD N	18 47 72
USB_IR	USB_90D	USB	USB IR P	
	USB_90D	USB	USB IR N	
USB_EXTB	USB_90D	USB	USB EXTB P	
	USB_90D	USB	USB EXTB N	
USB_T57	USB_90D	USB	USB T57 P	
	USB_90D	USB	USB T57 N	
USB_EXTC	USB_90D	USB	USB EXTC P	9 18
	USB_90D	USB	USB EXTC N	9 18
USB_SDCARD	USB_90D	USB	USB SDCARD P	18 38
	USB_90D	USB	USB SDCARD N	18 38
USB_WM	USB_90D	USB	USB WM P	
	USB_90D	USB	USB WM N	
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP USB RBIAS GND	18
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP 0 CLK	19 42
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP 0 DATA	19 42
(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP 1 CLK	19 42
(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP 1 DATA	19 42
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK	7 19 37
	HDA_55S	HDA	HDA BIT CLK R	19
HDA_SYNC	HDA_55S	HDA	HDA SYNC	7 19 37
	HDA_55S	HDA	HDA SYNC R	19
HDA_RST_L	HDA_55S	HDA	HDA RST R L	19
	HDA_55S	HDA	HDA RST L	7 19 37
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	7 19 37
	HDA_55S	HDA	HDA SDIN CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT	7 19 37
	HDA_55S	HDA	HDA SDOUT R	19
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP HDA PULLDN COMP	19
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK R	19 25
	CLK_SLOW_55S	CLK_SLOW	PM CLK32K SUSCLK	25 39
SPI_CLK	SPI_55S	SPI	SPI CLK R	19 41
	SPI_55S	SPI	SPI CLK	41
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	19 41
	SPI_55S	SPI	SPI MOSI	41
SPI_MISO	SPI_55S	SPI	SPI MISO	19 41
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	19 41
	SPI_55S	SPI	SPI CS0 L	41
	SPI_55S	SPI	SPI MLB CLK	41 48
	SPI_55S	SPI	SPI MLB MOSI	41 48
	SPI_55S	SPI	SPI MLB MISO	41 48
	SPI_55S	SPI	SPI MLB CS L	41 48
	SPI_55S	SPI	SPI ALT CLK	7 41
	SPI_55S	SPI	SPI ALT MOSI	7 41
	SPI_55S	SPI	SPI ALT MISO	7 41
	SPI_55S	SPI	SPI ALT CS L	7 41

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
MCP Constraints 2

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

PAGE 103 OF 110

SHEET 69 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

SD Card Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

RGMII Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	9 18
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	9 18
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0>	9 18
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	9 18
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	9 18
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	
	ENET_MII_55S	ENET_MII	ENET_RESET_L	

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SD_DATA	SD_55S	SD_INTERFACE	SD_D<4..0>	7 38
	SD_55S	SD_INTERFACE	SDCONN_DATA<4..0>	
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<4>	
SD_DATA_R	SD_55S	SD_INTERFACE	SD_D<7..5>	7 38
	SD_55S	SD_INTERFACE	SDCONN_DATA<7..5>	
	SD_55S	SD_INTERFACE	BCM57765_CR_DATA<7..5>	
SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	7 38
	SD_55S	SD_INTERFACE	SD_CLK_R	38
	SD_55S	SD_INTERFACE	SDCONN_CLK	
SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	7 38
	SD_55S	SD_INTERFACE	SDCONN_CMD	
	SD_55S	SD_INTERFACE	BCM57765_CR_CMD	

NOTE: SD_D<7..5> are different to support BCM5764M/BCM57765 co-layout.

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
Ethernet Constraints

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

PAGE 104 OF 110

SHEET 70 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	42
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	42
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	42
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	42
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	42
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	42
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	7 42
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	7 42
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	42
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	51
	1TO1_DIFFPAIR		CHGR_CSI_N	51
	1TO1_DIFFPAIR		CHGR_CSI_R_P	51
	1TO1_DIFFPAIR		CHGR_CSI_R_N	51
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	51
	1TO1_DIFFPAIR		CHGR_CSO_N	51
	1TO1_DIFFPAIR		CHGR_CSO_R_P	44 51
	1TO1_DIFFPAIR		CHGR_CSO_R_N	44 51

SYNC_MASTER=K99_MLB SYNC_DATE=04/08/2010

PAGE TITLE
SMC Constraints

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

PAGE 106 OF 110

SHEET 71 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=1:1_SPACING	?
AUDIO	*	=1:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SD CARD READER LAYOUT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S OVERRIDE	* OVERRIDE	OVERRIDE	=STANDARD OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_P	36 69
(USB_EXTA)	USB_90D	USB	USB_EXTA_MUXED_N	36 69
(USB_EXTA)	USB_90D	USB	USB_LT1_P	36
(USB_EXTA)	USB_90D	USB	USB_LT1_N	36
(USB_TPAD)	USB_90D	USB	USB_TPAD_P	18 47 69
(USB_TPAD)	USB_90D	USB	USB_TPAD_N	18 47 69
(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_P	7 47
(USB_TPAD)	USB_90D	USB	USB_TPAD_CONN_N	7 47
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	I2C_SMC_SMS_SDA_R	
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	I2C_SMC_SMS_SCL_R	
	SMB_55S	SMB	I2C_TCON_SCL	42
	SMB_55S	SMB	I2C_TCON_SDA	42
	SMB_55S	SMB	I2C_TCON_SCL_CONN	60
	SMB_55S	SMB	I2C_TCON_SDA_CONN	60

Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_90D	DISPLAYPORT	DP_INT_ML_P<1..0>	9 60
	DP_90D	DISPLAYPORT	DP_INT_ML_N<1..0>	9 60
	DP_90D	DISPLAYPORT	DP_INT_ML_C_P<1..0>	60
	DP_90D	DISPLAYPORT	DP_INT_ML_C_N<1..0>	60
	DP_90D	DISPLAYPORT	DP_INT_ML_F_P<1..0>	7 60
	DP_90D	DISPLAYPORT	DP_INT_ML_F_N<1..0>	7 60
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_C_P	7 60
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_C_N	7 60
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_P	9 60
	DP_90D	DISPLAYPORT	DP_INT_AUX_CH_N	9 60
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP_EXT_ML_P<3..0>	9 62
	DP_90D	DISPLAYPORT	DP_EXT_ML_N<3..0>	9 62
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_P<3..0>	62
	DP_90D	DISPLAYPORT	DP_EXT_ML_C_N<3..0>	62
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_P<3..0>	62
	DP_90D	DISPLAYPORT	DP_EXT_ML_F_N<3..0>	62
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_P	9 62
	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH_C_N	9 62

Power Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPUTHMSNS_D2	THERM_1TO1_55S	THERM	DRAMTHMSNS_D2_P	45
	THERM_1TO1_55S	THERM	DRAMTHMSNS_D2_N	45
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 45
	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 45
MCPTHMSNS_D2	THERM_1TO1_55S	THERM	MLBR_THMDIODE_P	45
	THERM_1TO1_55S	THERM	MLBR_THMDIODE_N	45
MCP_THMDIODE	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	19 45
	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	19 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	43 53
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	43 53
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	34 43
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	34 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CSREG_P	44
	SENSE_1TO1_55S	SENSE	ISNS_CSREG_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	35 43
	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	35 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	43 63
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_P	56
	SENSE_1TO1_55S	SENSE	CPUVTTS0_CS_N	56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	IMVP6_CS_P	54
	SENSE_1TO1_55S	SENSE	IMVP6_CS_N	54
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	IMVP6_CS_R_P	54
	SENSE_1TO1_55S	SENSE	IMVP6_CS_R_N	54
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VTTSENSE_P	56
	SENSE_1TO1_55S	SENSE	CPU_VTTSENSE_N	56
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_P	22 55
	SENSE_1TO1_55S	SENSE	MCPCORES0_VSEN_N	22 55
		MEM_POWER	PP1V5R1V35_S3	7 8
		SB_POWER	PP3V3_S5	7 8 58
		SB_POWER	PP3V3_S0	7 8 58
		SB_POWER	PP1V5_S0	7 8 58
		GND	GND	

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P	7 37 49
	DIFFPAIR	AUDIO	SPKRAMP_INR_N	7 37 49
MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P	49
	DIFFPAIR	AUDIO	MAX98300_R_N	49

SYNC_MASTER=T27_MLB SYNC_DATE=09/08/2009

PAGE TITLE
K16/K99 Specific Constraints

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

PAGE 108 OF 110

SHEET 72 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL3,ISL10	Y	0.250 MM	0.250 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.250 MM	0.250 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.140 MM	0.140 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.090 MM	0.090 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.076 MM	0.076 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.125 MM	0.125 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
75_OHM_DIFF	TOP,BOTTOM	Y	0.160 MM	0.160 MM		0.160 MM	0.160 MM
75_OHM_DIFF	ISL3,ISL10	Y	0.120 MM	0.120 MM		0.140 MM	0.140 MM
75_OHM_DIFF	ISL4,ISL9	Y	0.140 MM	0.140 MM		0.140 MM	0.140 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
95_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
95_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM			0.210 MM
95_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL3,ISL10	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.28:1_SPACING	*	0.228 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NB_STATIC	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
1.5X_DIELECTRIC	*	0.105 MM	?
5X_DIELECTRIC	*	0.350 MM	?

SYNC MASTER=K99_MLB SYNC DATE=04/08/2010

PAGE TITLE: K99 RULE DEFINITIONS

Apple Inc.

DRAWING NUMBER: 051-8467 SIZE: D

REVISION: 3.3.0

BRANCH:

PAGE: 109 OF 110

SHEET: 73 OF 74

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7980	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF
138S0632	9	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF
138S0633	9	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF
138S0634	9	CAP, 2.2UF, 6.3V, 20%, 0402	[illegible]	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C[illegible]	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9486,C2500,C2520,C2560,C2567,C2600,C[illegible]	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C[illegible]	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9486,C2500,C2520,C2560,C2567,C2600,C[illegible]	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4690,C4695,C5025,C7205,C7290,C7345,C7355,C[illegible]	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C9012,C9486,C2500,C2520,C2560,C2567,C2600,C[illegible]	CRITICAL	TY_CAP_10UF

22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0635	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	SS_CAP_22UF
138S0635	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	SS_CAP_22UF
138S0635	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	SS_CAP_22UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0676	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	MU_CAP_22UF
138S0676	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	MU_CAP_22UF
138S0676	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	MU_CAP_22UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0688	4	CAP, 22UF, 6.3V, 20%, 0603	C1210,C1214,C1217,C1218	CRITICAL	TY_CAP_22UF
138S0688	3	CAP, 22UF, 6.3V, 20%, 0603	C1223,C1226,C1227	CRITICAL	TY_CAP_22UF
138S0688	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	TY_CAP_22UF

SYNC_MASTER=K16_MLB SYNC_DATE=06/01/2010

PAGE TITLE
Acoustic Cap BOM Config Tables

Apple Inc.

DRAWING NUMBER 051-8467 SIZE D

REVISION 3.3.0

BRANCH

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED